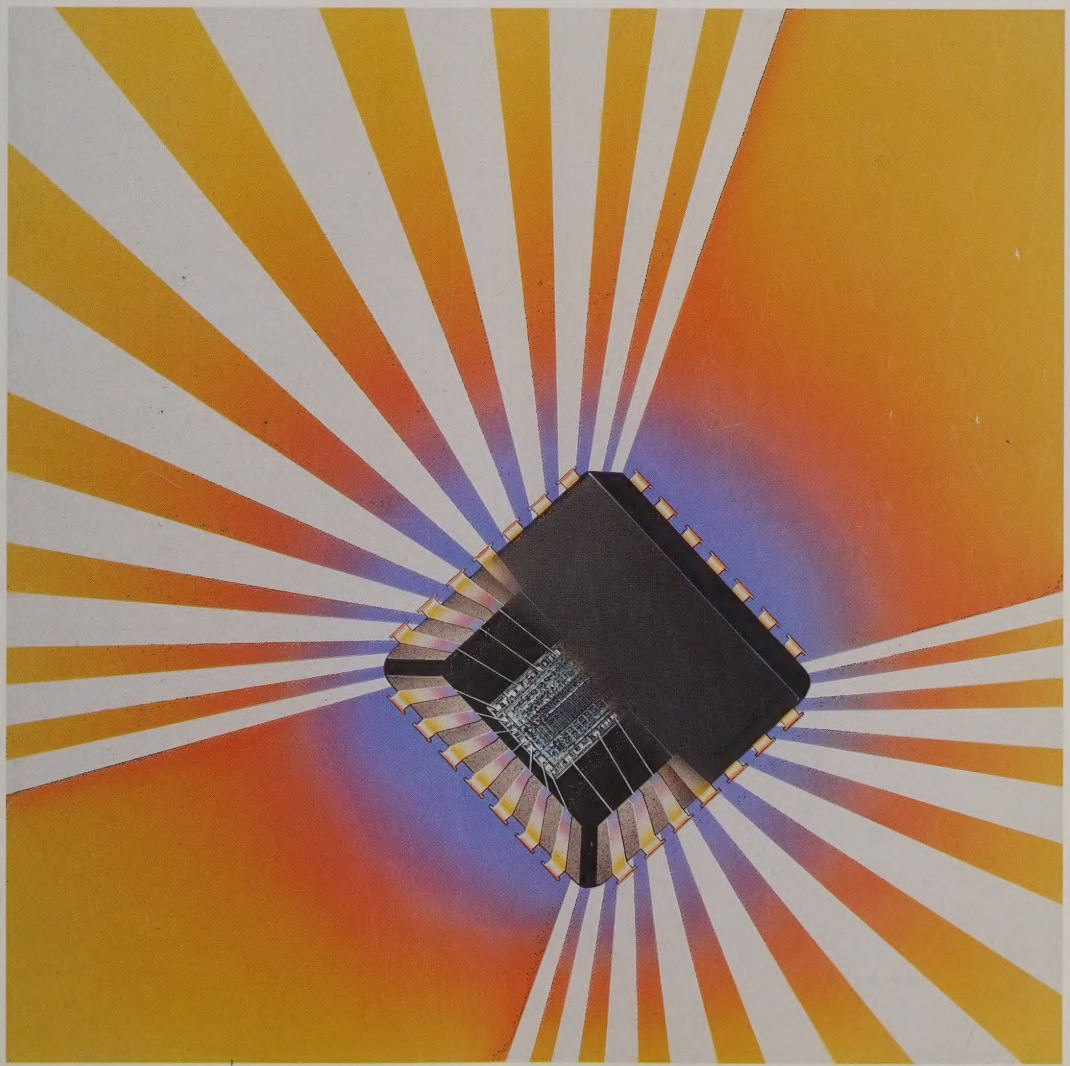
PAL® Device Data Book

1992

Advanced
Micro
Devices



Family	Part Number	Standard Packages	Technology	Features	t_{PD} ns	I_{CC} mA	Page
UNIVERSAL PAL DEVICES							
16V8	PALCE16V8H-7 PALCE16V8H-10** PALCE16V8Q-15 PALCE16V8H-15** PALCE16V8Q-25 PALCE16V8H-25**	20P, J 20S**	EE CMOS	GAL® Device Equivalent	7.5 10 15 15 25 25	115 115 55 90 55 90	2–48
	PALCE16V8Z-25	20P, J	EE CMOS	Zero Power	25†	0.015	2–75
	PALCE16VHD-15	24P, 28J	EE CMOS	High-Drive	15	115	2–91
18P8	AmPAL18P8B AmPAL18P8AL AmPAL18P8A AmPAL18P8L	20P, J	TTL	Comb., Prog. Polarity	15 25 25 35	180 90 180 90	2–111
20V8	PALCE20V8H-10 PALCE20V8Q-15 PALCE20V8H-15 PALCE20V8Q-25 PALCE20V8H-25	24P, 28J	EE CMOS	GAL Device Equivalent	10 15 15 25 25	115 55 90 55 90	2–172
22P10	AmPAL22P10B AmPAL22P10AL AmPAL22P10A	24P, 28J	TTL	Comb., Prog. Polarity	15 25 25	180 90 180	2–195
22V10	PAL22V10-7 PAL22V10-10 PAL22V10-15 AmPAL22V10A	24P, 28J	TTL	Varied Term Distribution	7.5 10 15 25	220 180 180 180	2–204
	PALCE22V10H-10 PALCE22V10H-15** PALCE22V10Q-25 PALCE22V10H-25**	24P, 28J 20S**	EE CMOS	Varied Term Distribution	10 15 25 25	130 90 55 90	2–232
	PALCE22V10Z-25	24P, 28J	EE CMOS	Zero Power	25†	0.015	2–253
24V10	PALCE24V10H-15 PALCE24V10H-25	28P, J	EE CMOS	28-Pin GAL-Type	15 25	115 115	2–267
26V12	PALCE26V12H-15 PALCE26V12H-20	28P, J	EE CMOS	28-Pin	15 20	105 105	2–282
29M16	PALCE29M16H-25	24P, J	EE CMOS	Advanced	25	100	2–297
ASYNCHRONOUS PAL DEVICES							
610	PALCE610H-15 PALCE610H-25	24P, 28J	EE CMOS	J-K F/Fs, Prog. CLK	15 25	90 90	2–344
20RA10	PALCE20RA10H-15	24P, 28J	EE CMOS	Prog. CLK	15	100	2–160
29MA16	PALCE29MA16H-25	24P, 28J	EE CMOS	Prog. CLK, Advanced Macrocell	25	100	2–319

† Industrial Grade

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PAL® Device

1992 Data Book

ADVANCED MICRO DEVICES

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For your high-density PLD requirements, please contact an AMD representative for our latest printing of the MACH™ Family Data Book.

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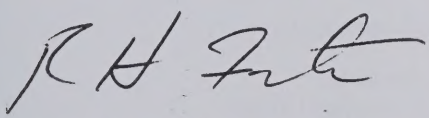
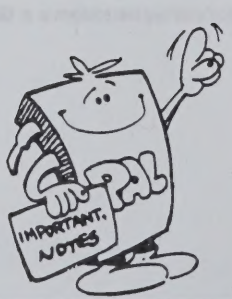


Rich Forte
Group Vice President
Programmable Products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CHAPTER 1
Introduction

Product Overview 1–3
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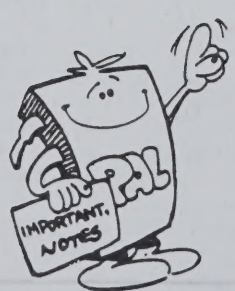
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Product Overview

Advanced Micro Devices offers the industry's widest variety of Programmable Logic Devices (PLDs), implemented in a variety of technologies. In this section, we will briefly discuss the device families, and look at the various architecture, speed, and power options. More specific device information can be found in the individual data sheets. Discussions on some of the special architectural features of many of the devices can also be found in their respective data sheets.

There are six basic PLD areas addressed by Advanced Micro Devices' PLDs:

- High-speed PAL® devices
- Universal PAL devices
- Industry-standard PAL devices
- Low-power PAL devices
- Special architecture PLDs
- High density PLDs

The largest application area is that covered by the Programmable Array Logic (PAL) devices. There is a wide variety of PAL devices, ranging from simple devices that address general logic design problems to more sophisticated devices that deal with more complex problems.

Within the group of special architecture PLDs, there are asynchronous devices, featuring an architecture particularly well suited to implementing asynchronous design functions optimally.

The final area, that of high-density design, is addressed by the MACH™ devices which provide a PLD with thousands of gates and very high performance. The Macro Array CMOS High-density (MACH) devices are described briefly in this section; for more detail, please refer to the MACH Data Book.

HIGH-SPEED PAL DEVICES

AMD offers the fastest PAL devices on the market today. We were the first to introduce the PAL device in 1978 and have been the first to market with volumes on all successive generations. As the market leader in the PLD arena, we fully expect to introduce even faster devices in the future.

Currently, we have the bipolar TTL PAL16R8 family of 20-pin devices in 5-ns speed grade and the PAL20R8 family of 24-pin devices, also in 5-ns speed grade, available in volume production. For extra performance we also have the 16R8 family at 4.5 ns, when packaged with the high-performance 28-pin PLCC pinout. These families include, both registered (16R4, 16R6, 16R8, 20R4, 20R6, 20R8) and combinational devices (16L8, 20L8). They are used in a wide variety of applications where performance and space are critical, often replacing FAST™ and AS SSI/MSI logic circuits. For applications where the absolute fastest devices are not needed, other speed grades are offered at a lower cost and/or lower power consumption.

AMD's Electronically Erasable (EE) CMOS process also provides high-speed universal PAL devices. The PALCE16V8 has a 7.5-ns version; most other EE CMOS devices have a 10- or 15-ns t_{PD}, while using half or even a quarter of the power required by their bipolar equivalents.

High-Speed PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PAL16L8	20	6	10	—	—	8	—	7	-4	4.5	125	210
PAL16R8	20	—	8	8	8	—	—	8	-5	5.0	117	210
PAL16R6	20	2	8	6	6	2	—	7–8	-7	7.5	74	180
PAL16R4	20	4	8	4	4	4	—	7–8				
PALCE16V8	20	0–8	8–10	8–0	—	—	8	7–8	H-7	7.5	100	115
PAL20L8	24	6	14	—	—	8	—	7	-5	5.0	117	210
PAL20R8	24	—	12	8	8	—	—	8				
PAL20R6	24	2	12	6	6	2	—	7–8	-7	7.5	74	210
PAL20R4	24	4	12	4	4	4	—	7–8				
PALCE20V8	24	0–8	12–14	8–0	—	—	8	7–8	H-10	10	55.5	115
PALCE24V10	28	0–10	14–16	10–0	—	—	10	7–8	H-15	15	45.5	115
PALCE22V10	24	0–10	12	10–0	—	—	10	8–16	H-10	10	83.3	130
PAL22V10	24	0–10	12	10–0	—	—	10	8–16	-7	7.5	91	220
PALCE610	24	0–16	4	16–0	—	—	16	8	H-15	15	45.5	90

*f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback.

UNIVERSAL PAL DEVICES

Have your design needs included a non-standard mix of inputs and outputs or choosing a variable number of combinatorial/registered/latched inputs and/or outputs for the given application? How about stocking only one or two PLDs to reduce your inventory costs?

The solution to your problem is AMD's family of universal PAL devices. We pioneered the concept of user-programmable output logic macrocells with the PAL22V10. With this macrocell, you can configure an output for combinatorial or registered operation and active-low or active-high polarity. This is what makes the PAL22V10 universal, for it can substitute for virtually all of the standard 24-pin PAL devices on the market. The PALCE26V12 is a 28-pin version which provides more inputs and outputs for those designs that don't quite fit into a PAL22V10.

But we did not stop there. A second new feature pioneered with the PAL22V10 is variable product term distribution; the 10 outputs on this device are arranged in pairs with 16, 14, 12, 10 or eight product terms on each output. With up to 16 product terms, the PAL22V10 can implement far more complex logic functions than can be supported by other 24-pin devices. No wonder the PAL22V10 is the most popular PAL device on the market today. And now both faster (7.5 ns, 91 MHz) and reprogrammable low-power CMOS (10 ns at 130 mA; 25 ns at 55 mA) versions are available from AMD.

The PALCE16V8 and PALCE20V8 are EE CMOS universal devices that have the additional capability of directly taking the designs of standard 20- and 24-pin PAL devices, respectively. They provide a cost-effective means of reducing inventory, lowering power, and reducing risk. The PALCE24V10 extends this architecture to 28 pins.

The PALCE610 adds to the basic macrocell by providing 16 I/O macrocells that can be configured with D, T, J-K, or S-R flip-flops.

The PALCE29M16 further enhances the macrocell concept. Its macrocell can be an input or an output macrocell that can be configured three ways: combinatorial, latched or registered. Sixteen of these macrocells are available in a 24-pin 300-mil package. And eight of the macrocells can be buried, allowing the connecting pins to be used as dedicated inputs. The PALCE29M16 also offers variable product term distribution.

For those applications where registers and latches are not needed, the AmPAL18P8 (20 pins) and AmPAL22P10 (24 pins) are ideal. These PAL devices with programmable polarity can flexibly replace almost all standard 20- and 24-pin combinatorial PAL devices. As a result, they significantly reduce your inventory. They are available in several speed-power grades to meet most application requirements.

Universal PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PALCE16V8	20	0–8	8–10	8–0	—	—	8	7–8	H-7	7.5	100	115
									H-10	10	55.5	115
									Q-15	15	45.5	55
									H-15	15	45.5	90
									Q-25	25	37	55
									H-25	25	37	90
									Z-25	25	40	0.015
PALCE20V8	24	0–8	12–14	8–0	—	—	8	7–8	H-10	10	55.5	115
									Q-15	15	45.5	55
									H-15	15	45.5	90
									Q-25	25	37	55
									H-25	25	37	90
PALCE24V10	28	0–10	14–16	10–0	—	—	10	7–8	H-15	15	45.5	90
									H-25	25	37	90
PALCE22V10	24	0–10	12	10–0	—	—	10	8–16	H-10	10	83.3	130
									H-15	15	50	90
									Q-25	25	33.3	55
									H-25	25	33.3	90
									Z-25	25	33.3	0.015
PAL22V10	24	0–10	12	10–0	—	—	10	8–16	-7	7.5	91	220
									-10	10	71	180
									-15	15	50	180
									A	25	28.5	180
PALCE20RA10	24	10	10	—	—	—	10	4	H-15	15	50	100
PALCE26V12	28	0–12	14	12–0	—	—	12	8–16	H-15	15	50	105
									H-20	20	40	105
PALCE610	24	0–16	4	16–0	—	—	16	8	H-15	15	45.5	90
									H-25	25	37	90
PALCE29M16	24	8–16	5	16–8	—	—	16	8–16	H-25	25	28.5	100
AmPAL18P8	20	8	10	—	—	8	—	8	B	15	—	180
									A	25	—	180
									AL	25	—	90
									L	35	—	90
AmPAL22P10	24	10	12	—	—	10	—	8	B	15	—	180
									A	25	—	180
									AL	25	—	90

*f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback.

INDUSTRY-STANDARD PAL DEVICES

As we have increased speed on the TTL PAL devices, we have also reduced the power consumption on the slower devices by as much as 75 percent. As a result, both the industry-standard 20-pin and 24-pin PAL device families are available in a variety of speed and power grades. This allows the designer to select the optimum performance at the lowest possible cost and power consumption. These 20-pin and 24-pin devices are used in applications where the advantages of reduced package count, such as higher reliability and lower power consumption, improve the overall price-performance of the end-product. Often these benefits are realized by replacing Schottky, ALS, LS and some CMOS SSI/MSI logic circuits with these PAL devices.

Standard PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PAL16L8	20	6	10	—	—	8	—	7	B	15	—	180
PAL16R8	20	—	8	8	8	—	—	8	B-2	25	25	90
PAL16R6	20	2	8	6	6	2	—	7–8	A	25	25	180
PAL16R4	20	4	8	4	4	4	—	7–8	B-4	35	16	55
PAL20L8	24	6	14	—	—	8	—	7	B	15	—	210
PAL20R8	24	—	12	8	8	—	—	8	B-2	25	25	105
PAL20R6	24	2	12	6	6	2	—	7–8	A	25	25	210
PAL20R4	24	4	12	4	4	4	—	7–8				

*f_{MAX} is defined as 1/(ts + tco) for the external feedback.

LOW-POWER PAL DEVICES

AMD is the only major supplier of programmable logic devices to offer a broad line of low-power CMOS devices. And we are the only PLD supplier with such a comprehensive CMOS programmable logic line.

There are two basic types of CMOS PAL devices: those that dissipate essentially no power when in a quiescent state, and faster devices which draw nominal current even when quiescent. Devices are thus classified as "zero-power" or "low-power."

Zero-power PAL devices are particularly suited for products that are portable or battery operated. In a standby mode they consume less than 15 µA. Low-power CMOS devices can cut system power consumption 50 percent by replacing equivalent 25-ns and 35-ns speed TTL PAL devices. By consolidating several SSI/MSI packages into a single CMOS PAL device, the power consumption can be cut even further.

Low-Power PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PALCE16V8	20	0–8	8–10	8–0	—	—	8	7–8	Z-25 Q-15	25 15	40 45.5	0.015 55
PALCE22V10	24	0–10	12	10–0	—	—	10	8–16	Z-25 Q-25	25 25	33.3 33.3	0.015 55

*f_{MAX} is defined as 1/(ts + tco) for the external feedback.

SPECIAL ARCHITECTURE PLDs

AMD offers a variety of programmable logic devices which have been enhanced architecturally to provide a high level of integration and performance. They consist of asynchronous devices which have been designed to implement asynchronous design functions optimally. These products offer you unprecedented flexibility in selecting the right PLD for the application at hand.

Asynchronous PAL Devices

Currently AMD makes three devices that are function specific. They support asynchronous and bus interface applications.

The PALCE20RA10 is optimized for asynchronous applications. It contains ten D-type flip-flops, driven by a PAL array. Each flip-flop has individually programmable Clock, Reset and Preset product terms. With such features, this device is well suited to replacing glue logic in your system.

The PALCE29MA16 combines some of the advantages of the PALCE29M16 with the advantages of the PALCE20RA10. It has one dedicated Clock/Latch Enable input as well as product terms for each of the 16 macrocells to allow individual clocking, asynchronous Reset and asynchronous Preset. It also features variable product term distribution. To top it off, the PALCE29MA16 is electrically reprogrammable in a plastic 300-mil package.

The PALCE610 is a general purpose PLD. It has 16 independently-configurable macrocells. Each macrocell can be configured as either combinatorial or registered. The registers can be D, T, J-K or S-R type flip-flops. The device has 4 dedicated input pins and 2 clock pins. Asynchronous clocking is available since each clock pin controls 8 of the 16 macrocells.

Asynchronous PAL Devices

Part Number	Functional Description								Commercial Specifications			
	Pin Count	Array Inputs			Array Outputs			Prod. Terms per Output	Spd/Pwr Options	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
		bidir.	dedctd.	reg. fdbk.	reg.	comb.	macrocell					
PALCE20RA10	24	10	10	—	—	—	10	4	H-15	15	50	100
PALCE29MA16	24	8–16	5	16–8	—	—	16	4–12	H-25	25	28.5	100
PALCE610	24	0–16	4	16–0	—	—	16	8	H-15 H-25	15 25	45.5 37	90 90

*f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback.

HIGH-DENSITY PLDs

For larger-scale integration, the MACH (Macro Array CMOS High-density) devices offer a breakthrough both in performance and cost. The architecture has been optimized to provide consistent, predictable 15-ns propagation delays (12 ns for the 44-pin devices), while keeping the cost per gate similar to that of a CMOS PAL device.

A MACH device looks like multiple PAL devices interconnected by a switch matrix. Because the switch matrix is fast, and because all signals have the same delays, every path provides a 15-ns delay from input to output.

Gate densities in the MACH family range from about 900 gates to about 3600 gates. The devices are made with electrically-erasable CMOS technology.

The MACH family pushes the PAL device concept to higher levels of integration that have been achieved efficiently before. Most PAL device design concepts still hold true. The number of third-party design tools that support the MACH devices makes it easy to migrate from PAL device design to MACH device design with little, if any, additional investment.

Further information on AMD's MACH product line may be found by obtaining the MACH Family Data Book (14051). MACH design assistance is available by obtaining the MACH Technical Briefs Manual (15972). Development assistance is available through the FusionPLD℠ Partners Catalog (15585).

MACH Devices

Device	Pins	Macrocells	Gate Equivalents	Max Inputs	Max Outputs	Max Flip-Flops	t_{PD} (ns)	f_{MAX}* (MHz)	I_{CC} (mA)
MACH 1 Family									
MACH110	44	32	900	38	32	32	15	50	150
MACH120	68	48	1200	58	48	48	20	40	180
MACH130	84	64	1800	70	64	64			180
MACH 2 Family									
MACH210	44	64	1800	38	32	64	15	50	180
MACH220	68	96	2400	58	48	96	20	40	–
MACH230	84	128	3600	70	64	128			–

*f_{MAX} is defined as $1/(t_S + t_{CO})$ for the external feedback.

Commercial PLDs for Industrial Applications

Customers have expressed an interest in using AMD programmable logic devices over the industrial temperature range. To serve your need, we recommend the following:

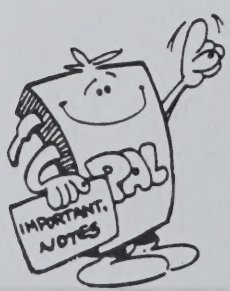
1. Use any standard commercial device from the following Family Data sheets:
   PALCE16V8
   PALCE20V8
   PALCE22V10
   PALCE610
2. Slow down all commercial timing parameters by 20%.
3. Add 20 mA to the commercial I_{CC}.

All standard AMD warranties will apply to products used as noted above at V_{CC} of +5 V ±10% over the temperature range of –40°C to 85°C.

This approach will allow you to use broadly available commercial devices to fill your industrial temperature needs at no price premium. We are able to assure the performance to specification of these products since they are characterized and monitored over the full military temperature range (–55°C to 125°C).

CHAPTER 2
PAL Device Data Sheets

PAL16R8 Family 2–3
PALCE16V8 Family 2–48
PALCE16V8Z-25 2–75
PALCE16V8HD-15 2–91
AmPAL18P8B/AL/A/L 2–111
PAL20R8 Family 2–121
PALCE20RA10H-15 2–160
PALCE20V8 Family 2–172
AmPAL22P10B/AL/A 2–195
PAL22V10 Family/AmPAL22V10/A 2–204
PALCE22V10 Family 2–232
PALCE22V10Z-25 2–253
PALCE24V10H-15/25 2–267
PALCE26V12H-15/20 2–282
PALCE29M16H-25 2–297
PALCE29MA16H-25 2–319
PALCE610 Family 2–344


PAL
IMPORTANT.
NOTES

Advanced Micro Devices

PAL16R8 Family

20-Pin TTL Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- **As fast as 4.5 ns maximum propagation delay**
- **Popular 20-pin architectures: 16L8, 16R8, 16R6, 16R4**
- **Programmable replacement for high-speed TTL logic**
- **Register preload for testability**
- **Power-up reset for initialization**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **20-pin DIP and PLCC packages save space**
- **28-pin PLCC-4 package provides ultra-clean high-speed signals**

GENERAL DESCRIPTION

The PAL16R8 Family (PAL16L8, PAL16R8, PAL16R6, PAL16R4) includes the PAL16R8-5/4 Series which provides the highest speed in the 20-pin TTL PAL device family, making the series ideal for high-performance applications. The PAL16R8 Family is provided with standard 20-pin DIP and PLCC pinouts and a 28-pin PLCC pinout. The 28-pin PLCC pinout contains seven extra ground pins interleaved between the outputs to reduce noise and increase speed.

The family utilizes Advanced Micro Devices' advanced trench-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. Once the PAL device is programmed and verified, an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.

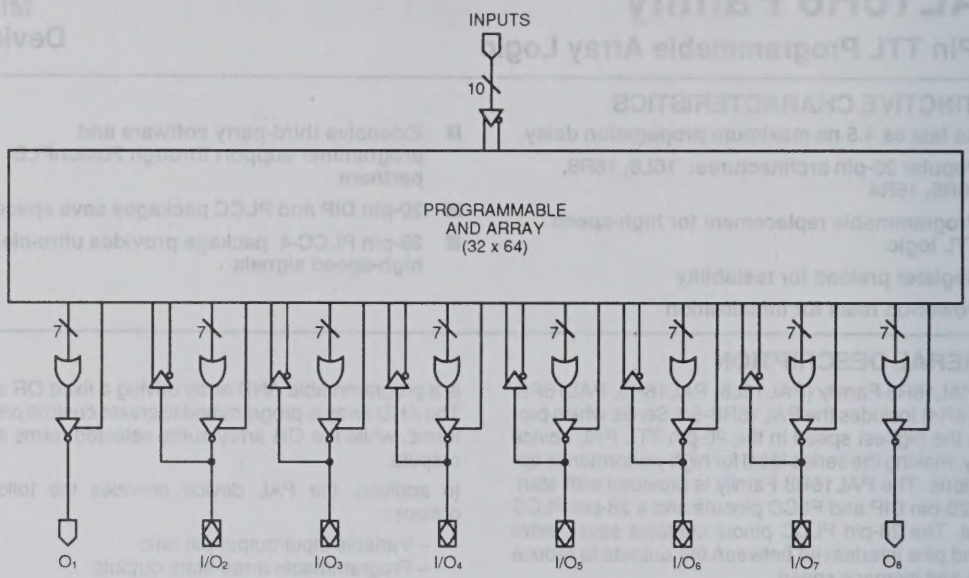
PRODUCT SELECTOR GUIDE

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL16L8	10	6 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL16R8	8	8 reg.	8	reg.	pin
PAL16R6	8	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL16R4	8	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

Publication# 16492 Rev. A Amendment/0
Issue Date: January 1992

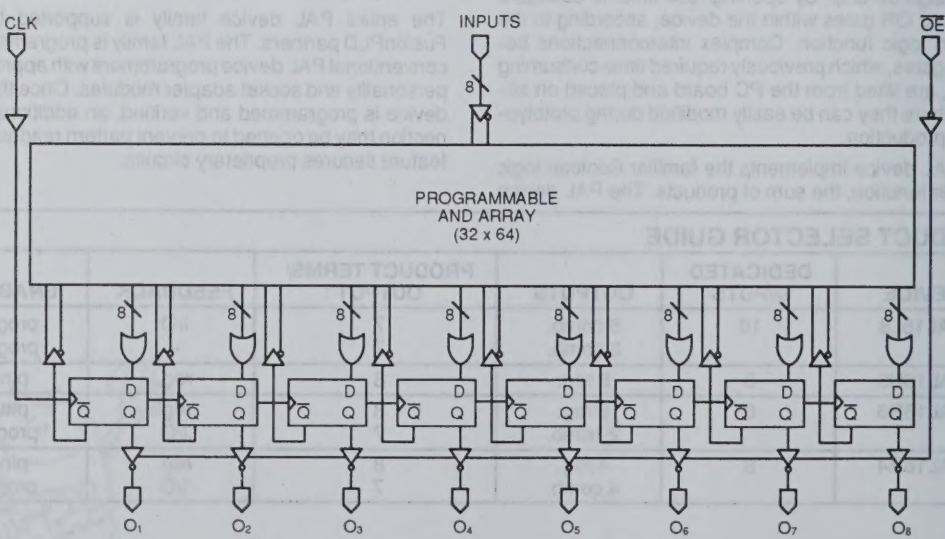
BLOCK DIAGRAMS

PAL16L8



12468-004A

PAL16R8



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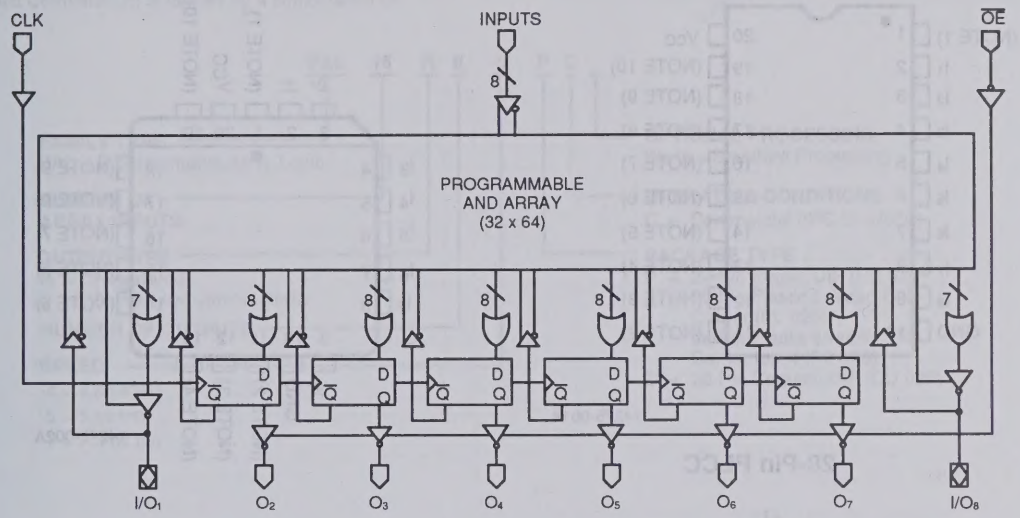
BLOCK DIAGRAMS

PAL16R6



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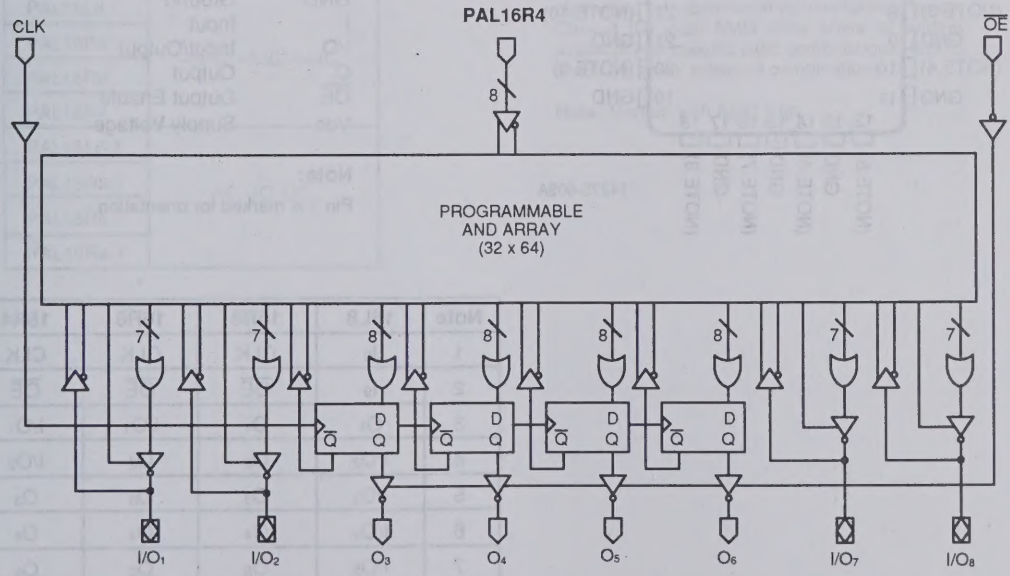
PAL16R4



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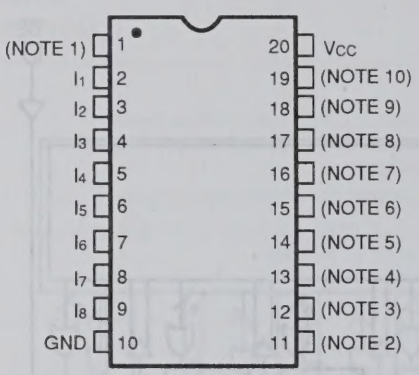
CONNECTION DIAGRAMS

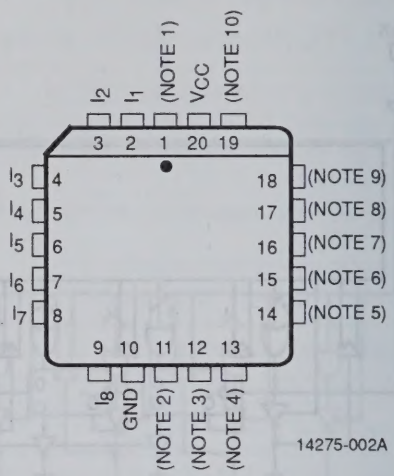
Top View

DIP



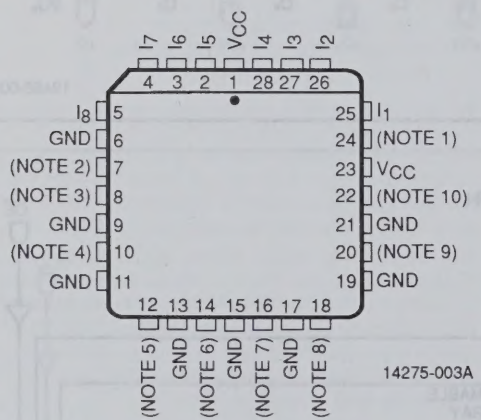
14275-001A

20-Pin PLCC



14275-002A

28-Pin PLCC



14275-003A

PIN DESIGNATIONS

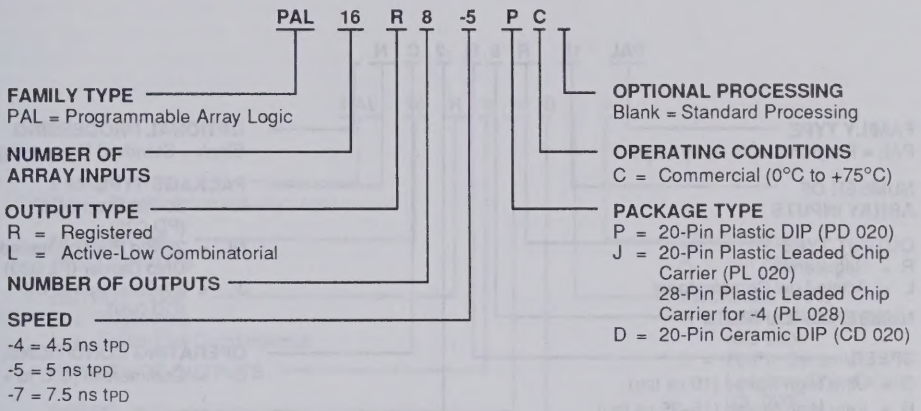
CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
O	Output
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

Note:
Pin 1 is marked for orientation.

Note	16L8	16R8	16R6	16R4
1	I_0	CLK	CLK	CLK
2	I_9	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	I/O_7
10	O_8	O_8	I/O_8	I/O_8

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL16L8	–5PC, –5JC, –4JC
PAL16R8	
PAL16R6	
PAL16R4	
PAL16L8-7	PC, JC, DC
PAL16R8-7	
PAL16R6-7	
PAL16R4-7	

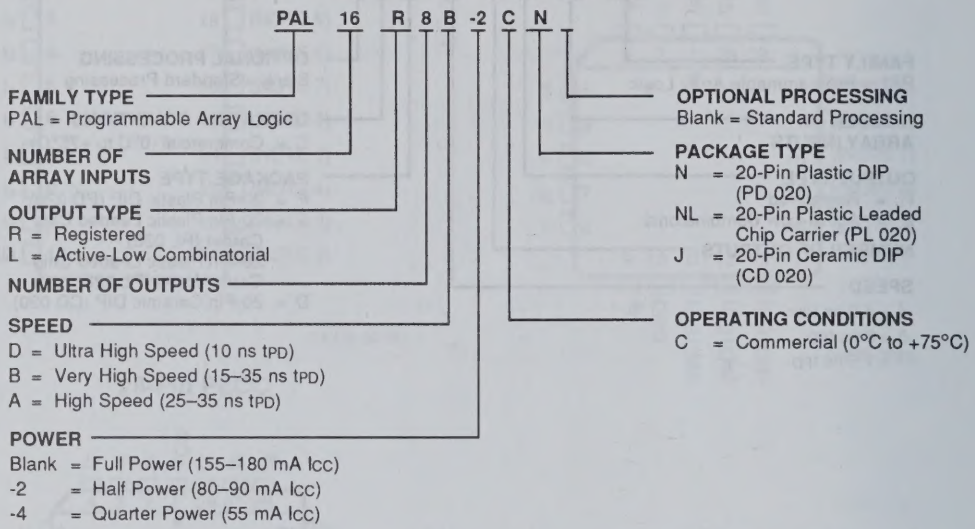
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION
Commercial Products (MMI Marking Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL16L8	D, B,	CN, CNL, CJ
PAL16R8	B-2, A,	
PAL16R6	B-4	
PAL16R4		

Valid Combinations

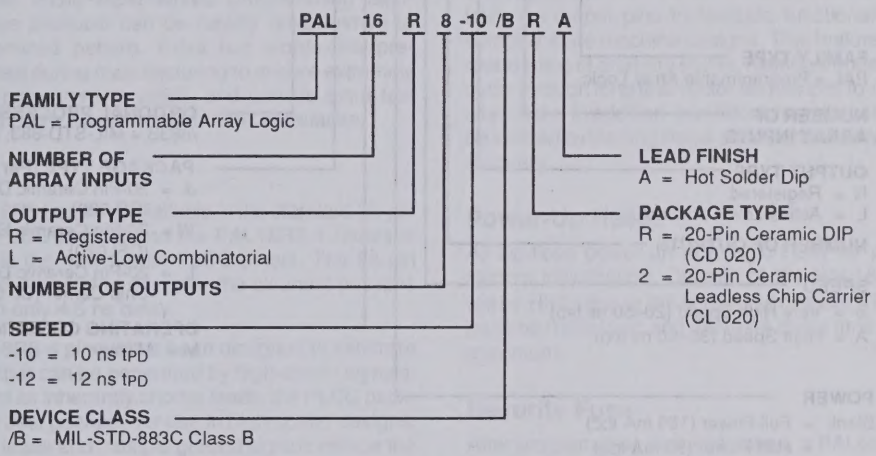
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL16L8	-10, -12	/BRA, /B2A
PAL16R8		
PAL16R6		
PAL16R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

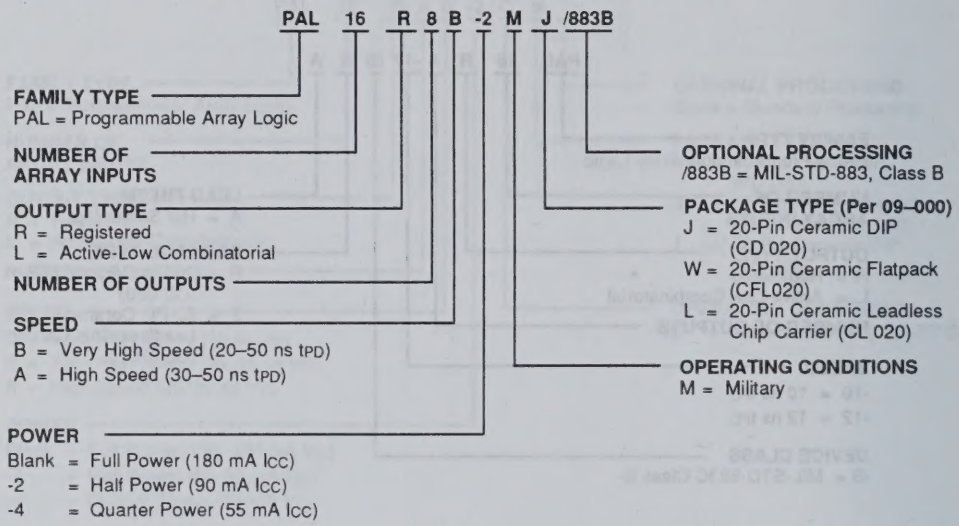
Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

ORDERING INFORMATION
APL Products (MMI Marking Only)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL16L8	B, B-2,	MJ/883B,
PAL16R8	A, B-4	MW/883B,
PAL16R6		ML/883B
PAL16R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional information on AMD's Standard Military grade products.

Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

Standard 20-pin PAL Family

The standard bipolar 20-pin PAL family devices have common electrical characteristics and programming procedures. Four different devices are available, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Pinouts

The PAL16R8 Family is available in the standard 20-pin DIP and PLCC pinouts and the PAL16R8-4 Series is available in the new 28-pin PLCC pinout. The 28-pin PLCC pinout gives the designer the cleanest possible signal with only 4.5 ns delay.

The PAL16R8-4 pinout has been designed to minimize the noise that can be generated by high-speed signals. Because of its inherently shorter leads, the PLCC package is the best package for use in high-speed designs. The short leads and multiple ground signals reduce the effective lead inductance, minimizing ground bounce. Placing the ground pins between the outputs optimizes the ground bounce protection, and also isolates the outputs from each other, eliminating cross-talk. This pinout can reduce the effective propagation delay by as much as 20% from a standard DIP pinout. Design files for PAL16R8-4 Series devices are written as if the device had a standard 20-pin DIP pinout for most design software packages.

Variable Input/Output Pin Ratio

The registered devices have eight dedicated input lines, and each combinatorial output is an I/O pin. The PAL16L8 has ten dedicated input lines and six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin and may be configured as a dedicated input if the output buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Register Preload

The register on the PAL16R8 Family can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL16R8 Family will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Security Fuse

After programming and verification, a PAL16R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The PAL16R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

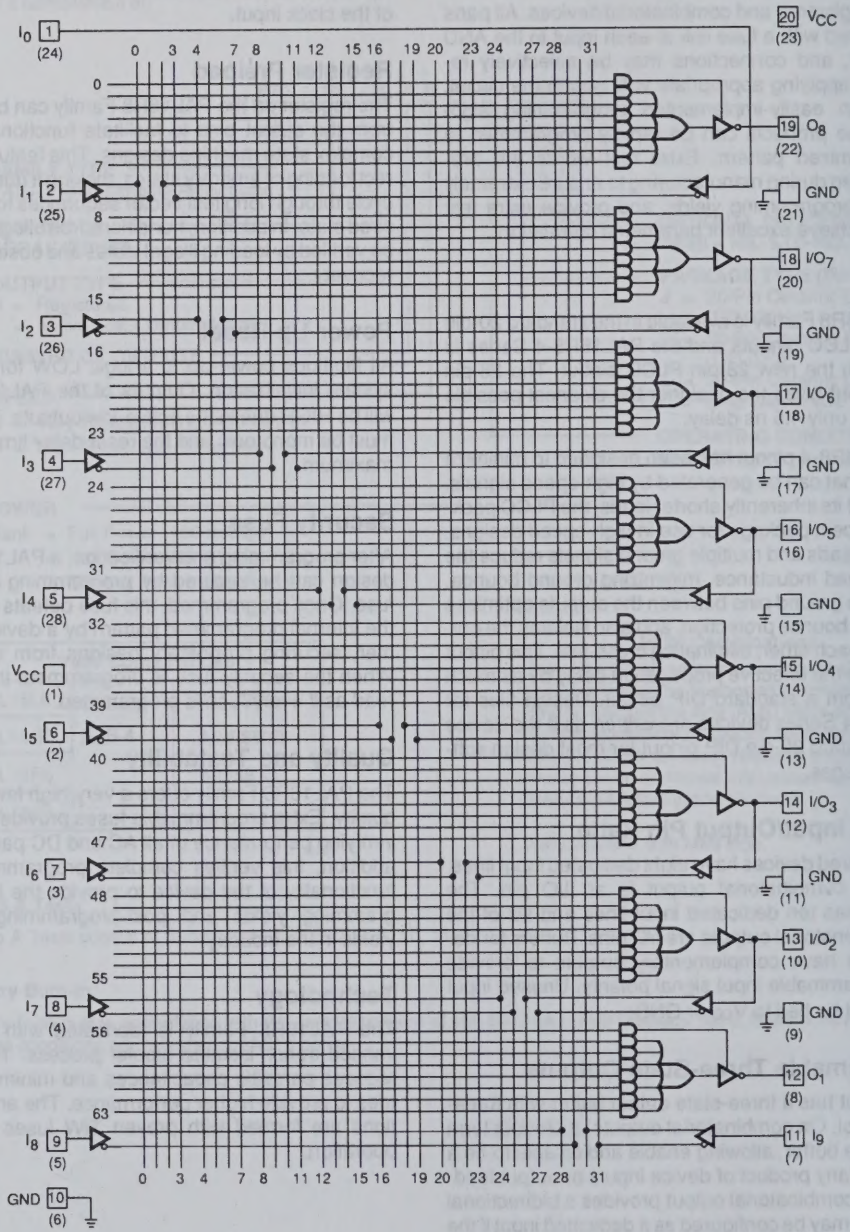
Technology

The PAL16R8 Family is fabricated with AMD's advanced trench-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses for reliable operation.

LOGIC DIAGRAM

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16L8 (-4)

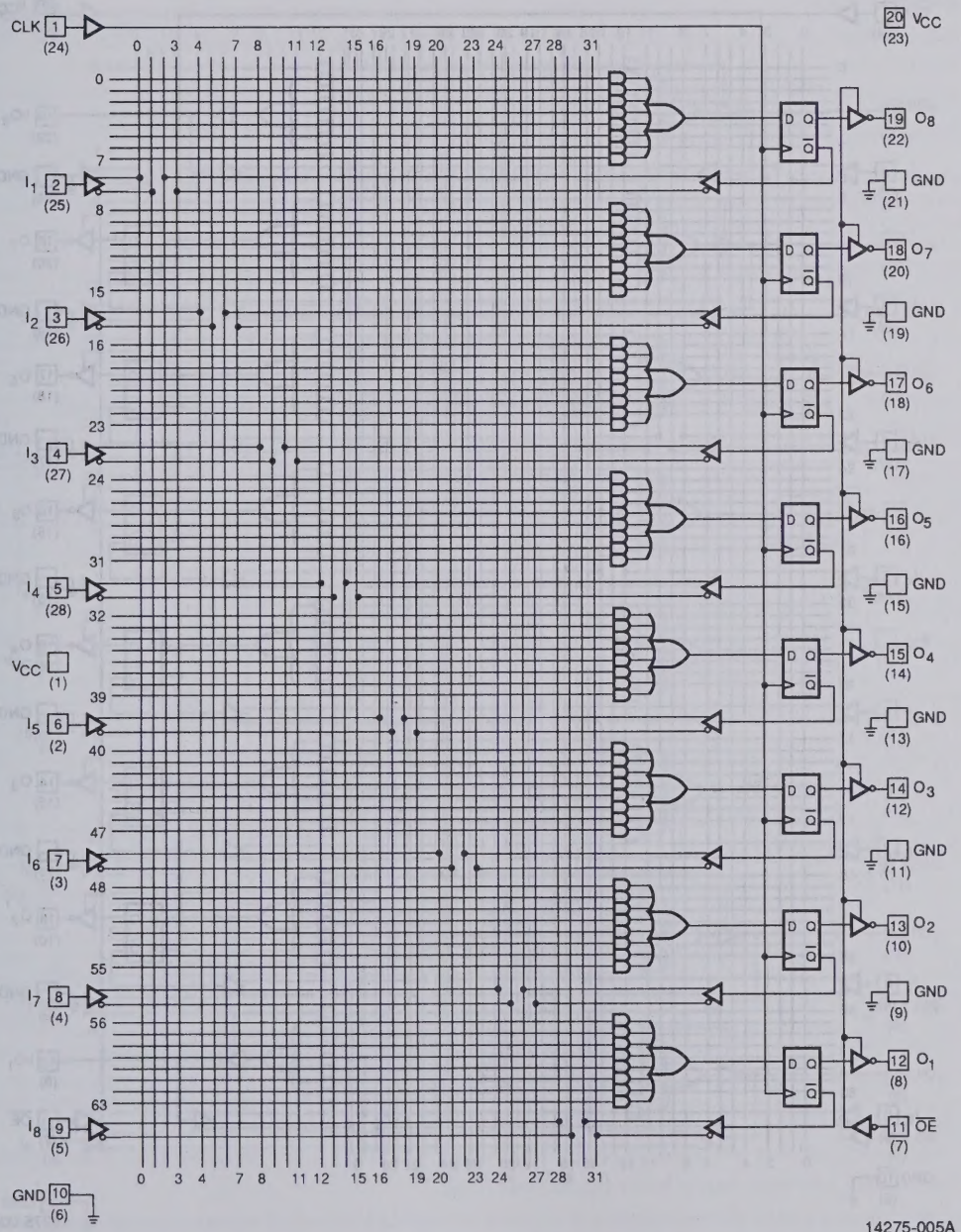


14275-004A

LOGIC DIAGRAM

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16R8 (-4)

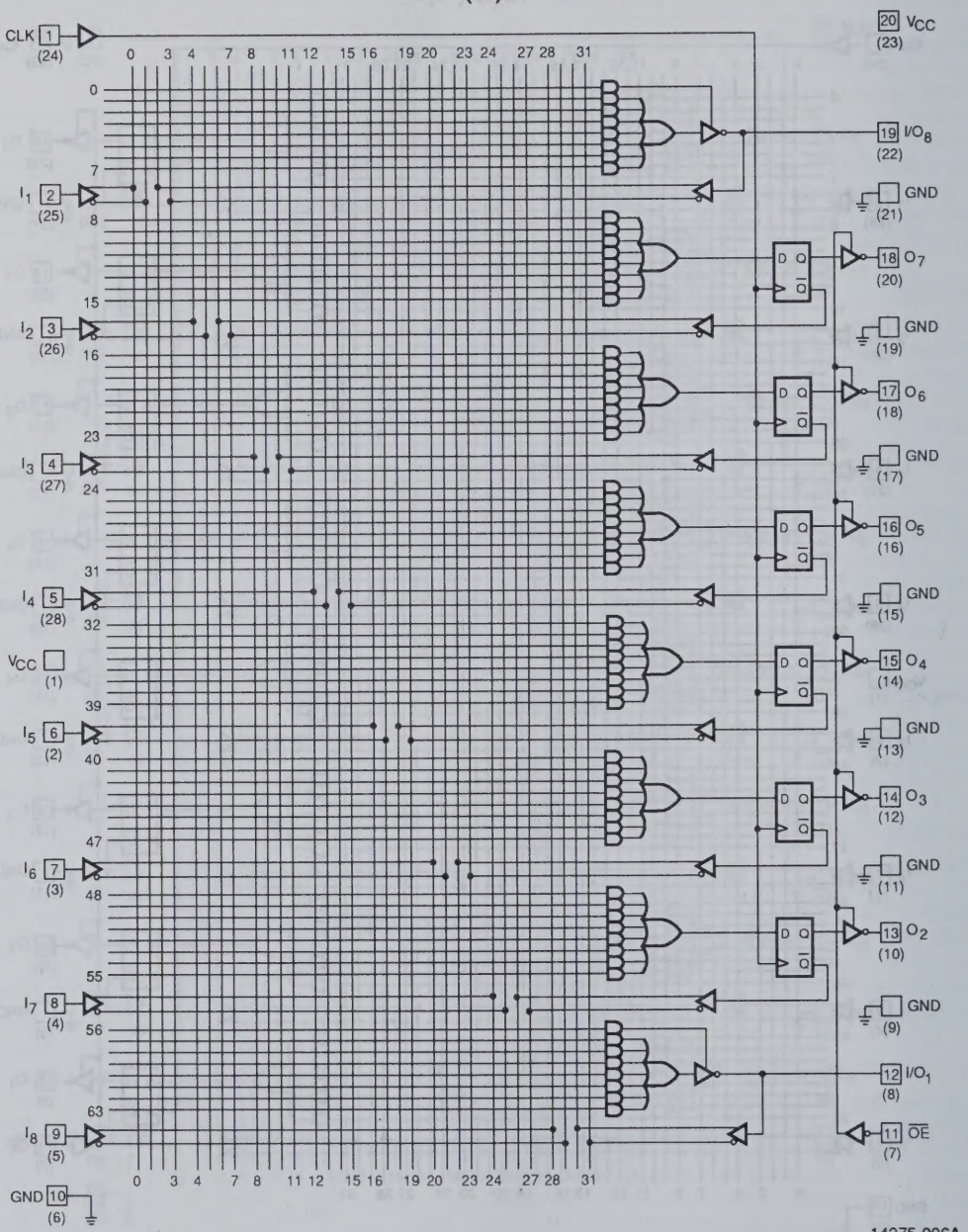


14275-005A

LOGIC DIAGRAM

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16R6 (-4)

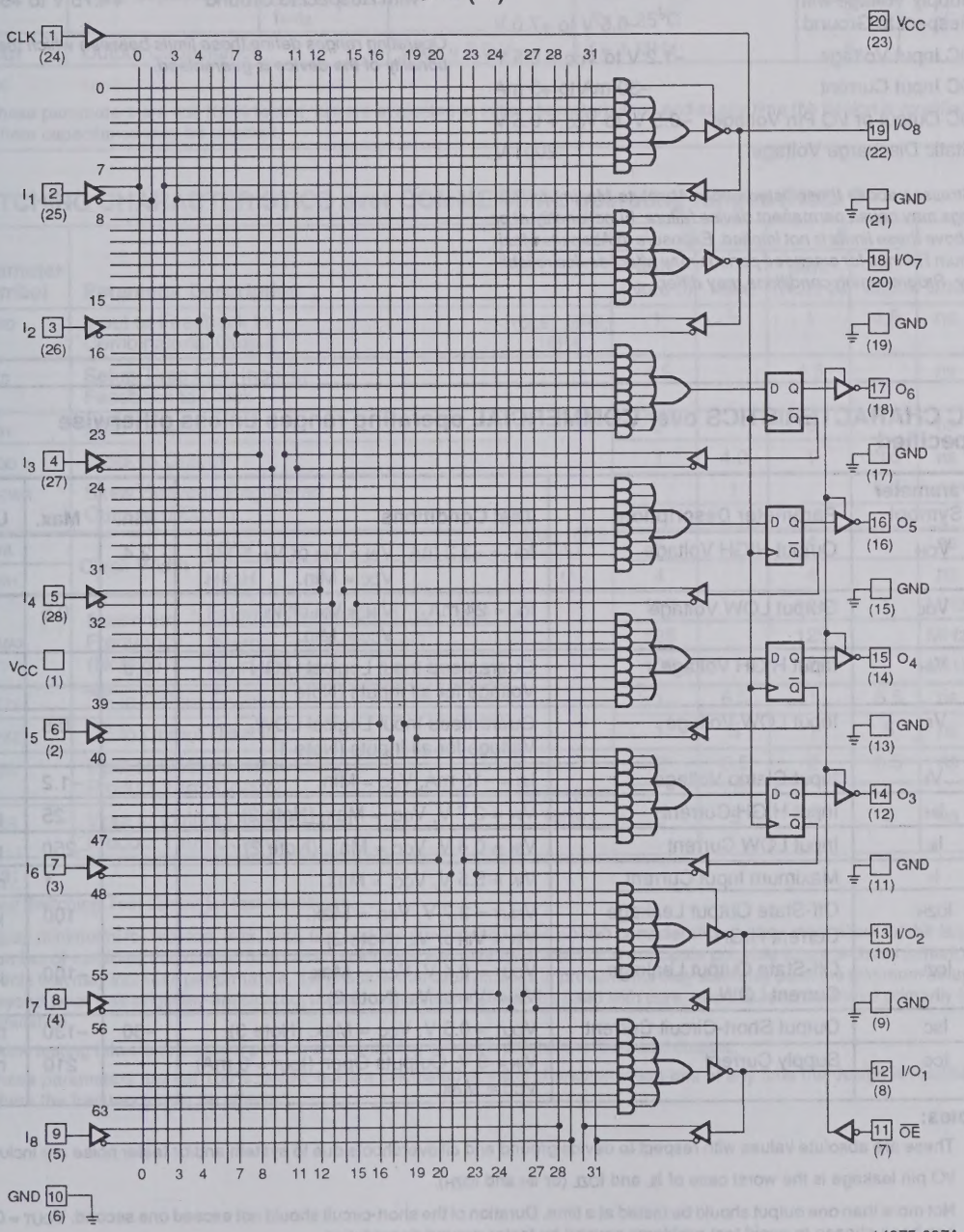


14275-006A

LOGIC DIAGRAM

DIP and 20-Pin PLCC (28-Pin PLCC) Pinouts

16R4 (-4)



14275-007A

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature with Power Applied	–65°C to +150°C
Storage Temperature	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to V_{CC} + 0.5 V
DC Input Current	–30 mA to +5 mA
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	CLK, $\overline{OE}$	V_{IN} = 2.0 V	V_{CC} = 5.0 V	8	pF
		I_1–I_8		T_A = 25°C	5	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-5 Min. (Note 3)	-5 Max.	-4 Min. (Note 3)	-4 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R8, 16R4	1	5	1	4.5	ns
t_S	Setup Time from Input or Feedback to Clock				4.5		4.5		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output				1	4.0	1	3.5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)					1		0.5	ns
t_{WL}	Clock Width	LOW		16R8, 16R6, 16R4	4		4		ns
t_{WH}		HIGH			4		4		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		117		125		MHz
		Internal Feedback (f_{CNT})			125		125		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		125		125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	6.5	1	6.5	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	5	1	5	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4	2	6.5	2	6.5	ns
t_{ER}	Input to Output Disable Using Product Term Control				2	5	2	5	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Delay minimums for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} are chosen based on two considerations: they must allow for the large number of variables that define "best case" conditions, and they must attempt to anticipate possible future process enhancements that may increase performance. It is possible that such process improvements may someday push the minimum delays beyond what was originally anticipated; therefore minimums should be used with care, and are recommended primarily for simulation.
4. Skew testing takes into account pattern and switching direction differences between outputs.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to +7.0 V
DC Input Current	–30 mA to +5 mA
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4	3	7.5	ns
		1 Output Switching			3	7	
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	7		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	6.5	ns
t_{SKEW}	Skew Between Registered Outputs (Note 4)					1	ns
t_{WL}	Clock Width	LOW			5		ns
t_{WH}		HIGH			5		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		74		MHz
		Internal Feedback (f_{CNT})			100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		100		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				3	8	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				3	8	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Skew is measured with all outputs switching in the same direction.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to +5.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	CLK, $\overline{OE}$	9	pF
				Other Inputs	2	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		Outputs	4	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4	3	10	ns
t_S	Setup Time from Input or Feedback to Clock				10		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				2	7	ns
t_{WL}	Clock Width	LOW			8		ns
t_{WH}		HIGH		16R8, 16R6,	8		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	1/(t_S + t_{CO})	16R4	58.8		MHz
		Internal Feedback (f_{CNT})			60		MHz
		No Feedback	1/(t_{WH} + t_{WL})		62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				3	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				3	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6,	1	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			16R4	1	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		15	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					12	ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					15	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4		15	ns
t_{ER}	Input to Output Disable Using Product Term Control					15	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		25	ns
t_S	Setup Time from Input or Feedback to Clock				25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{WL}	Clock Width	LOW		16R8, 16R6, 16R4	15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback (f_{CNT})			28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage		I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage		I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage		Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage		Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage		I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current		V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current		V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current		V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH		V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW		V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current		V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	16L8	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		155	mA
		16R8/6/4			180	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{CC} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback (f_{CNT})			28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −1 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−250	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		55	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V as been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		35	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	35		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		16		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					25	ns
t_{EA}	Input to Output Enable Using Product Term Control			16L8, 16R6, 16R4		35	ns
t_{ER}	Input to Output Disable Using Product Term Control					35	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to +5.5 V
DC Input Current	–30 mA to +5 mA
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Corner Pins	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	10	pF
		Middle Pins			5	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				-10 Min. (Note 3)	-10 Max.	-12 Min. (Note 3)	-12 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4	3	10	3	12	ns
t_S	Setup Time from Input or Feedback to Clock				10		10		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output				2	9	3	11	ns
t_{SKEW}	Skew Between Registered Outputs (Note 4)					1		1	ns
t_{WL}	Clock Width	LOW		16R8, 16R6, 16R4	8		8		ns
t_{WH}		HIGH			8		8		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		52.6		47.6		MHz
		Internal Feedback (f_{CNT})			60.6		60.6		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		62.5		62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 5)				1	10	1	12	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 5)				1	10	1	12	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)			16L8, 16R6, 16R4	1	10	1	12	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				1	10	1	12	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
4. Skew is measured with all outputs switching in the same direction.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to + 5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	−55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		10	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		20	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	20		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					15	ns
t_{WL}	Clock Width	LOW			12		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6, 16R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					20	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	−55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		90	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified ' where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		30	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW			20		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6, 16R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					30	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		7	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		30	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW			20		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)			16L8, 16R6, 16R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)					30	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–250	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		55	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

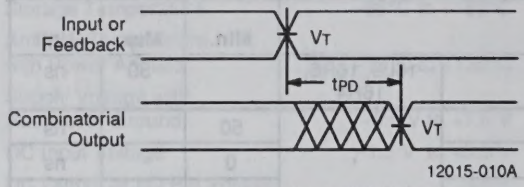
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			16L8, 16R6, 16R4		50	ns
t_S	Setup Time from Input or Feedback to Clock			16R8, 16R6, 16R4	50		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					25	ns
t_{WL}	Clock Width	LOW			25		ns
t_{WH}		HIGH			25		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		13.3		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			16L8, 16R6, 16R4		45	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					45	ns

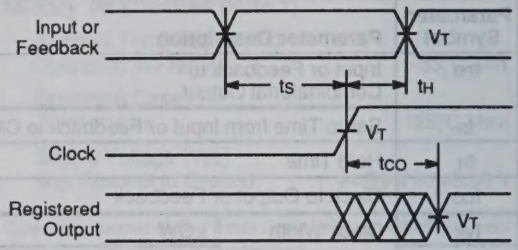
Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

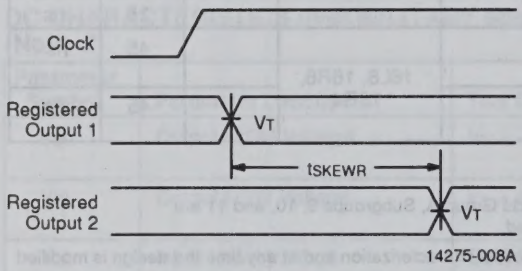
SWITCHING WAVEFORMS



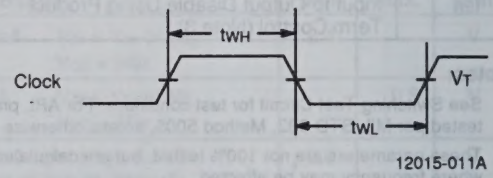
Combinatorial Output



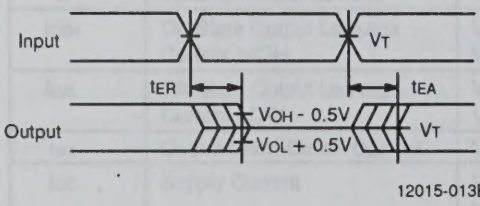
Registered Output



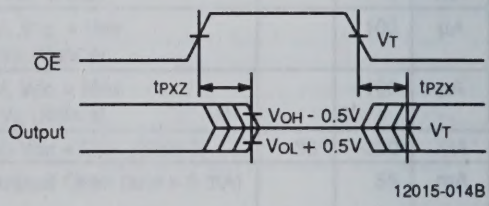
Registered Output Skew



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

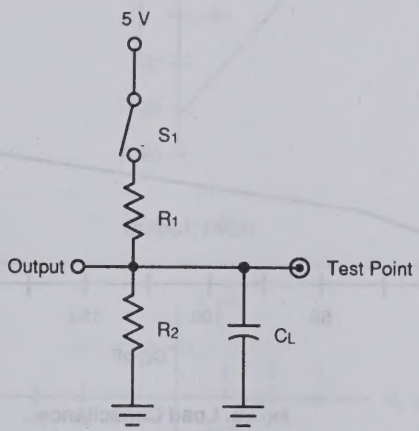
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–3 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

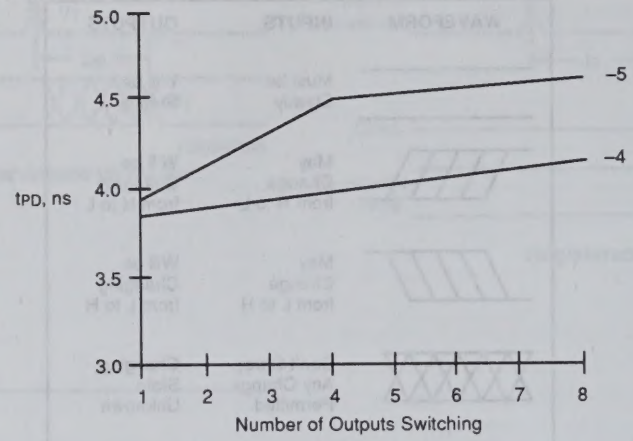


12350-019A

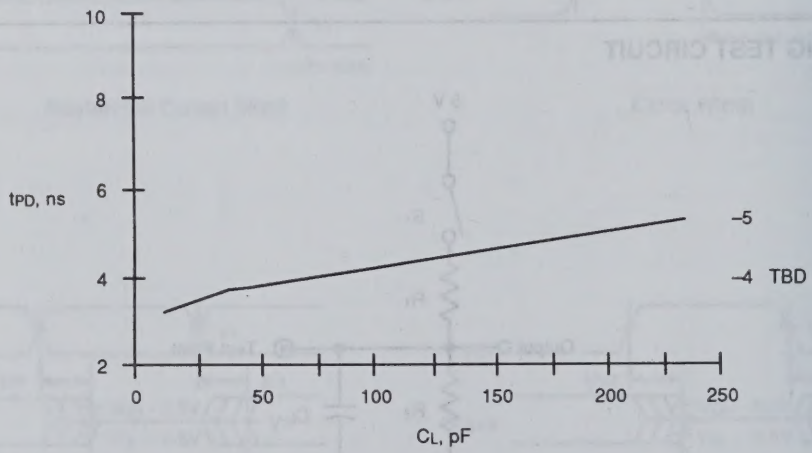
Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	200 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

MEASURED SWITCHING CHARACTERISTICS for the PAL16R8-4/5

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching 14275-010A



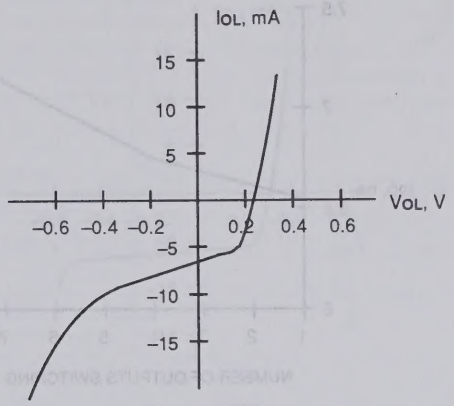
t_{PD} vs. Load Capacitance 14275-011A
V_{CC} = 5.25 V, T_A = 25°C

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.

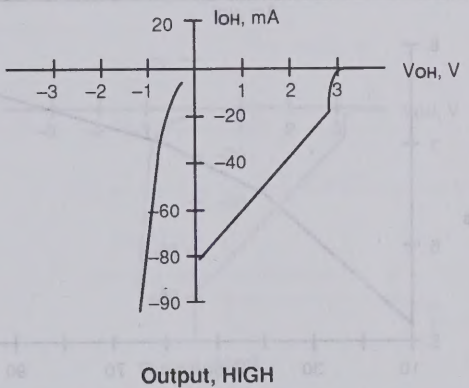
CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS for the PAL16R8-4/5

V_{CC} = 5.0 V, T_A = 25°C



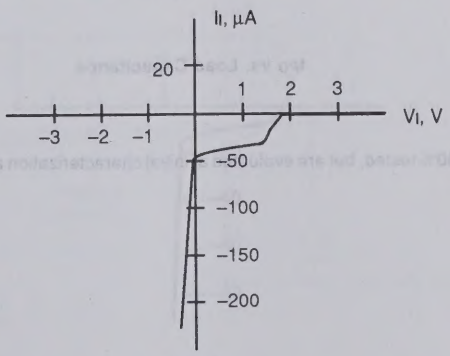
Output, LOW

10240-003B



Output, HIGH

10240-004B

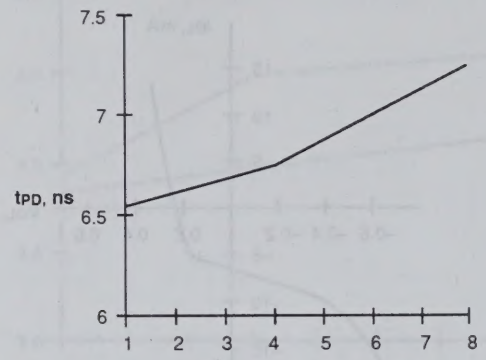


Input

10240-005A

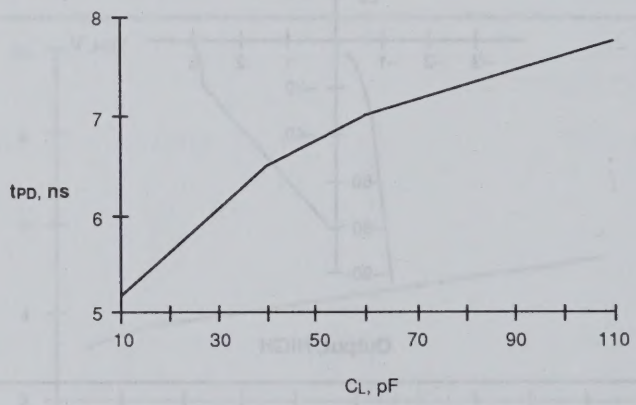
MEASURED SWITCHING CHARACTERISTICS for the PAL16R8-7

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching

10240-001A



t_{PD} vs. Load Capacitance

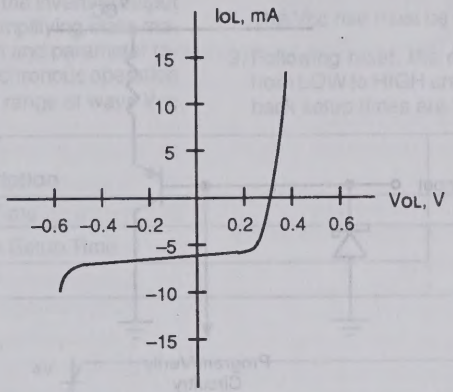
10240-002A

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.

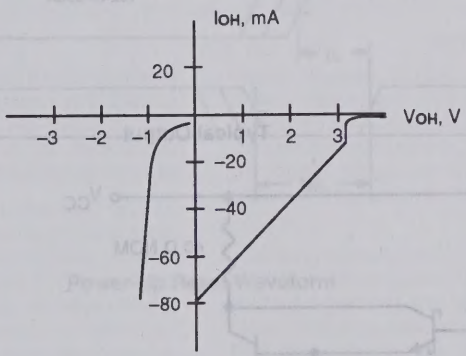
CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS for the PAL16R8-7

V_{CC} = 5.0 V, T_A = 25°C



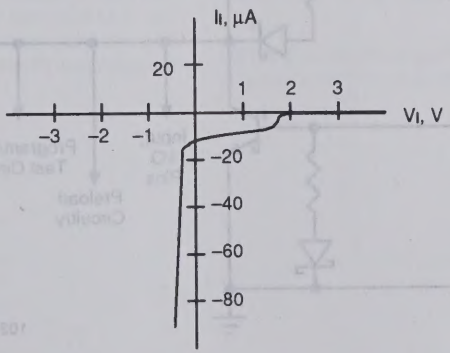
Output, LOW

10240-003A



Output, HIGH

10240-004A

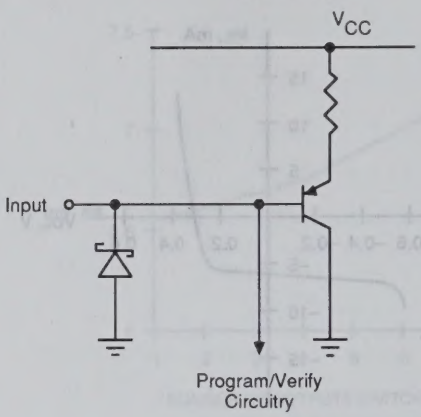


Input

10240-005A

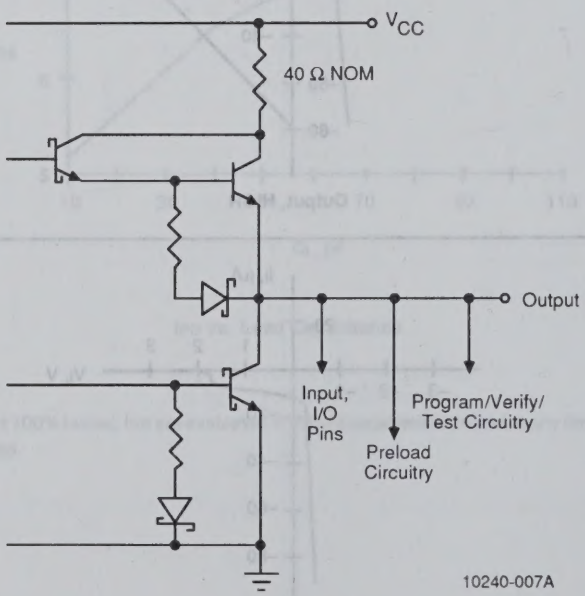
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



10240-006A

Typical Output



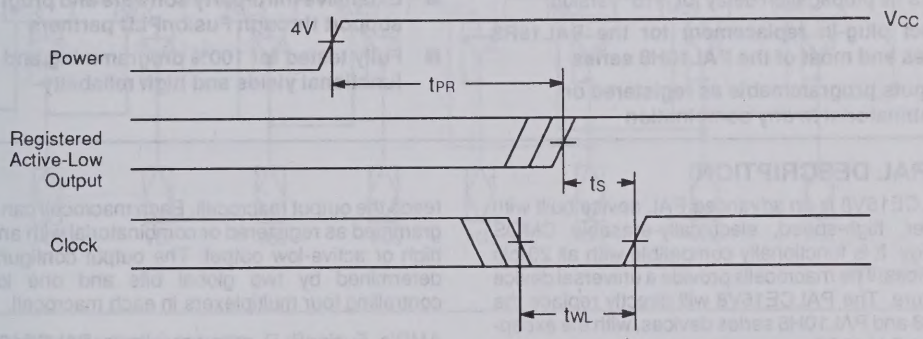
10240-007A

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

PALCE16V8 Family

EE CMOS 20-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Pin, function and fuse-map compatible with all 20-pin GAL® devices**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - 7.5 ns propagation delay for "-7" version
  - 10 ns propagation delay for "-10" version
  - 15 ns propagation delay for "-15" version
- **Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

The PALCE16V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8 will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

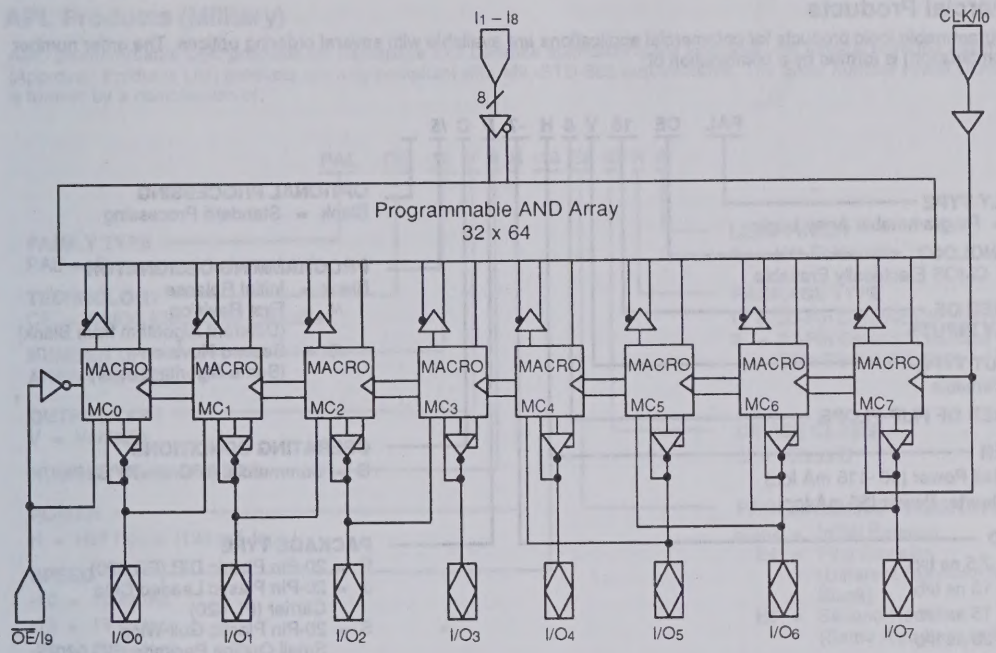
The PALCE16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE16V8 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 16493 Rev. A Amendment/0
Issue Date: January 1992

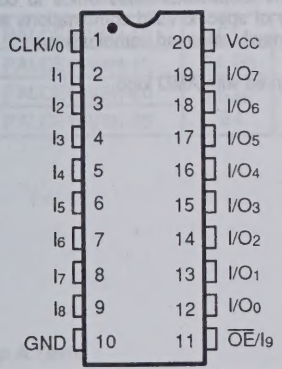
BLOCK DIAGRAM



12197-001B

CONNECTION DIAGRAMS
Top View

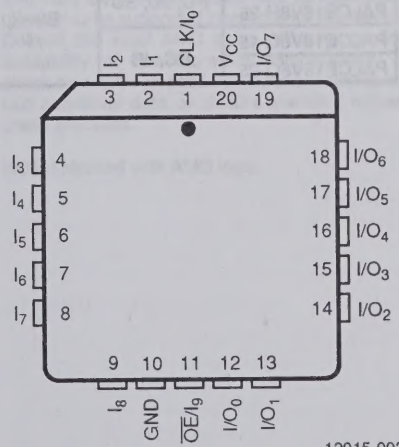
DIP/SOIC



12015-002A

Note: Pin 1 is marked for orientation

PLCC/LCC



12015-003A

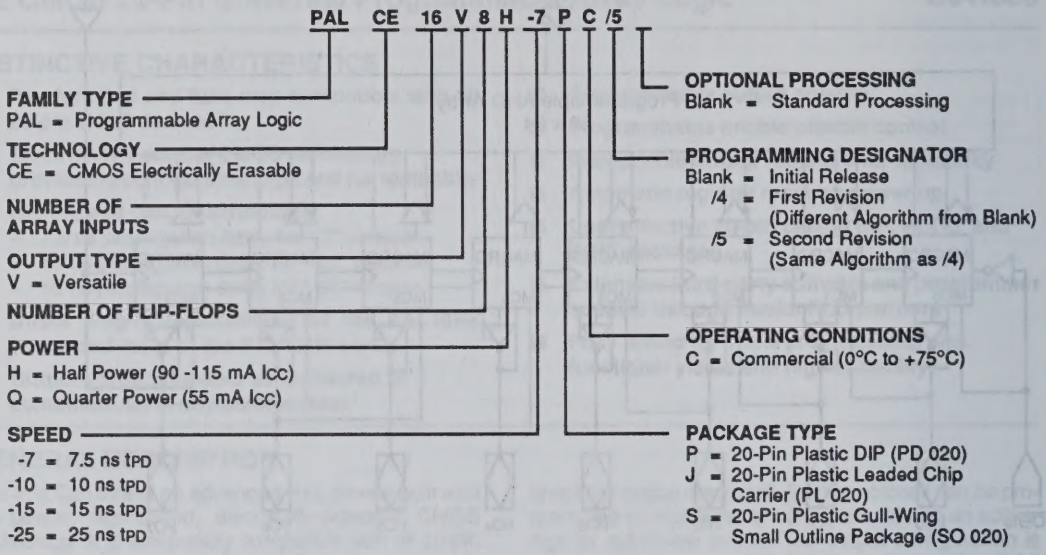
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
$\overline{OE}$ = Output Enable
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE16V8H-7	PC, JC	/5
PALCE16V8H-10	PC, JC, SC	/4, /5
PALCE16V8H-15	PC, JC, SC	Blank, /4
PALCE16V8H-25		
PALCE16V8Q-15	PC, JC	
PALCE16V8Q-25		

Valid Combinations

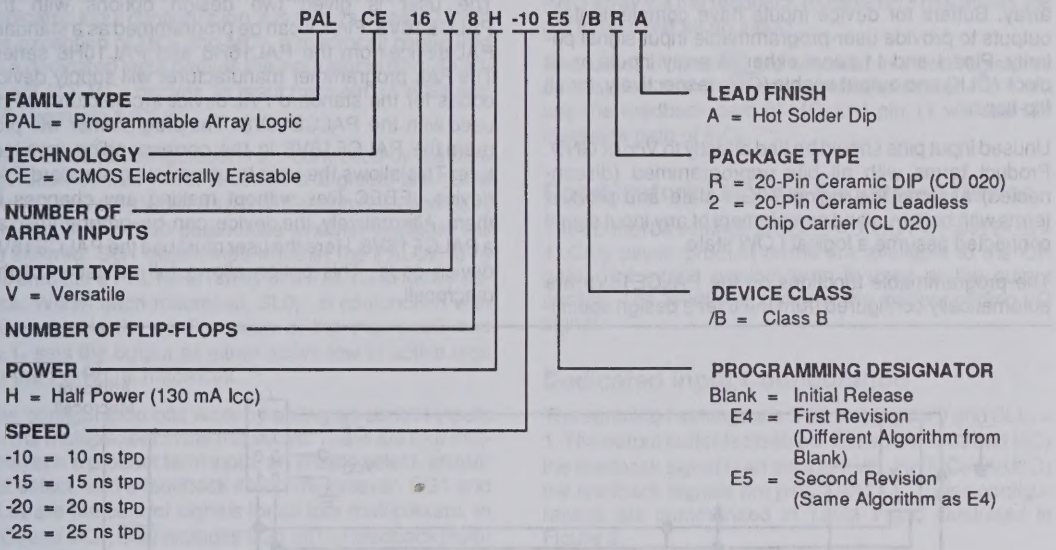
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION

APL Products (Military)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE16V8H-10	E5	/BRA /B2A
PALCE16V8H-15	E4, E5	
PALCE16V8H-20	Blank, E4	
PALCE16V8H-25		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-in

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

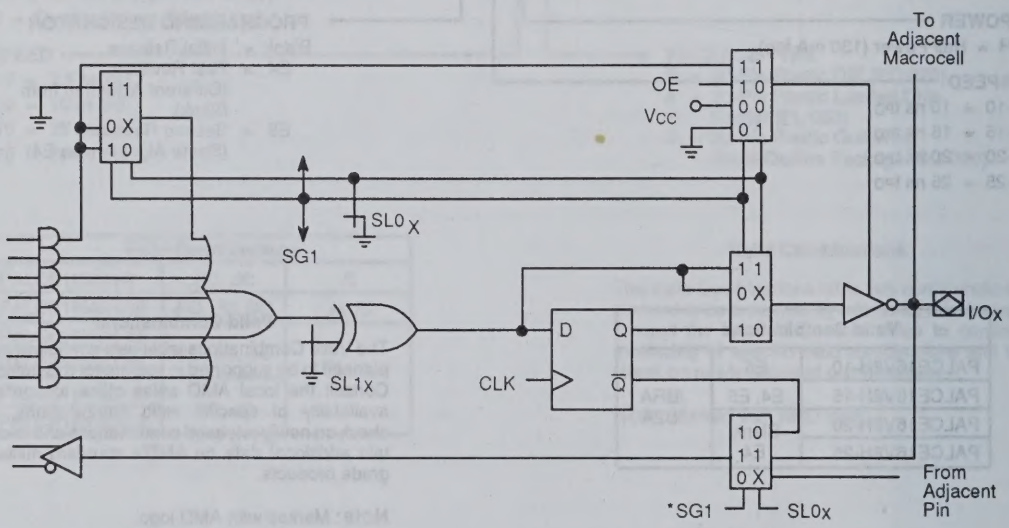
FUNCTIONAL DESCRIPTION

The PALCE16V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8. The programmer will program the PALCE16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8. Here the user must use the PALCE16V8 device code. This option allows full utilization of the macrocell.



*In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.

14408C-001A

PALCE16V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8 will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 15 and 16. Pins 15 and 16 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

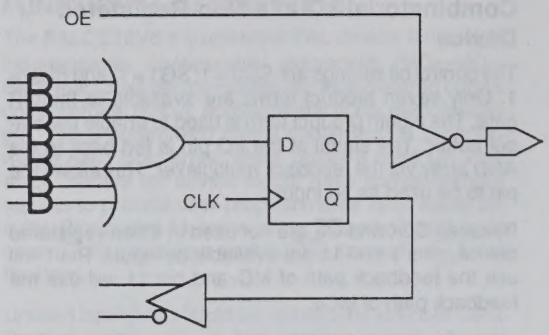
Table 1. Macrocell Configuration

SG0	SG1	$SL0_x$	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

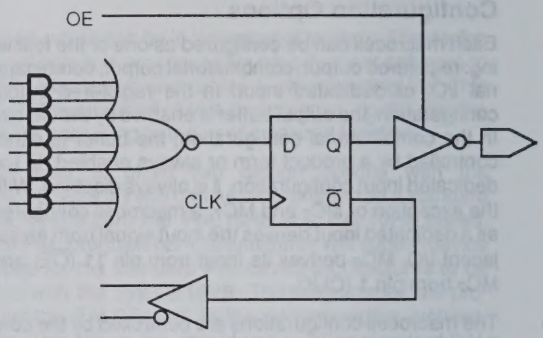
Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

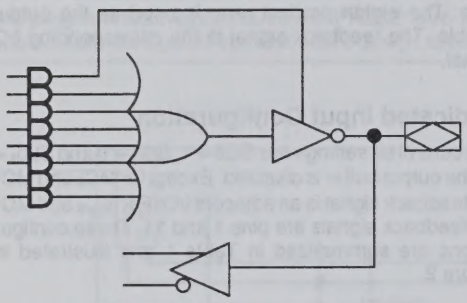
Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



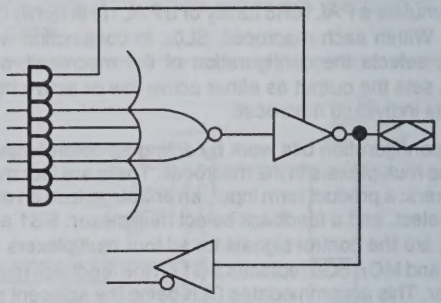
Registered Active Low



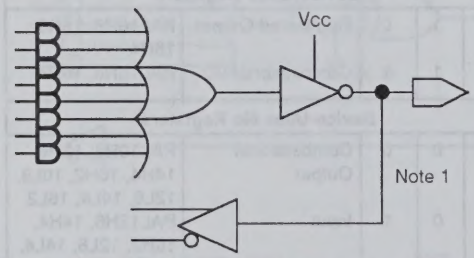
Registered Active High



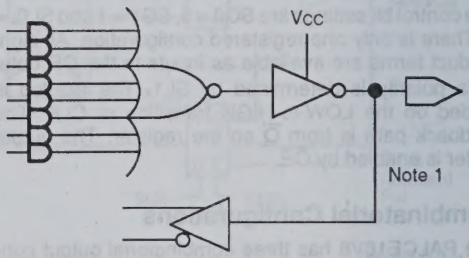
Combinatorial I/O Active Low



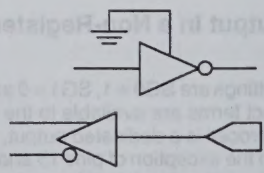
Combinatorial I/O Active High



Combinatorial Output Active Low



Combinatorial Output Active High



Dedicated Input

14408C-002A

Notes:

1. Feedback is not available on pins 15 and 16 in the combinatorial output mode.
2. This configuration is not available on pins 15 and 16.

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

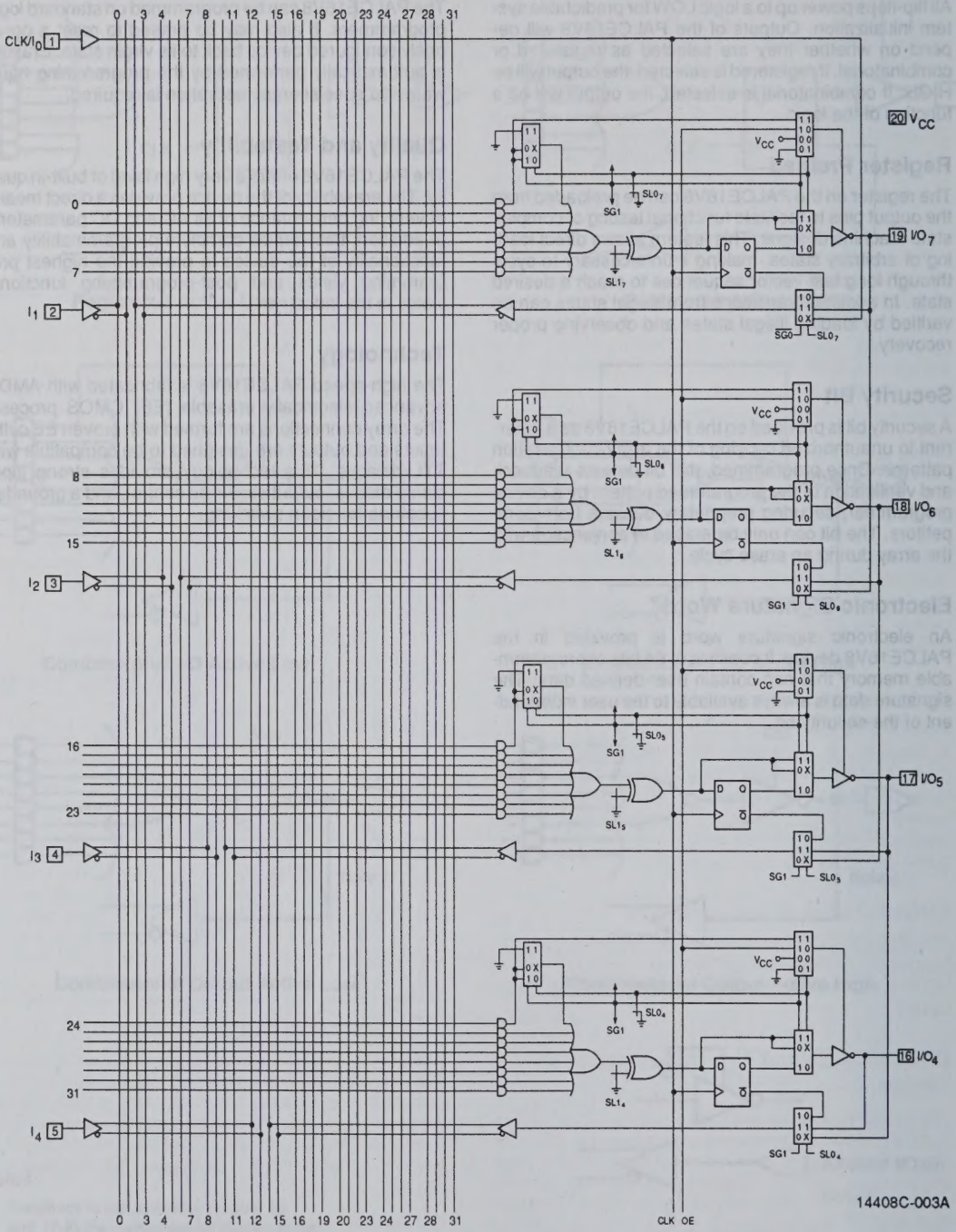
Quality and Testability

The PALCE16V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

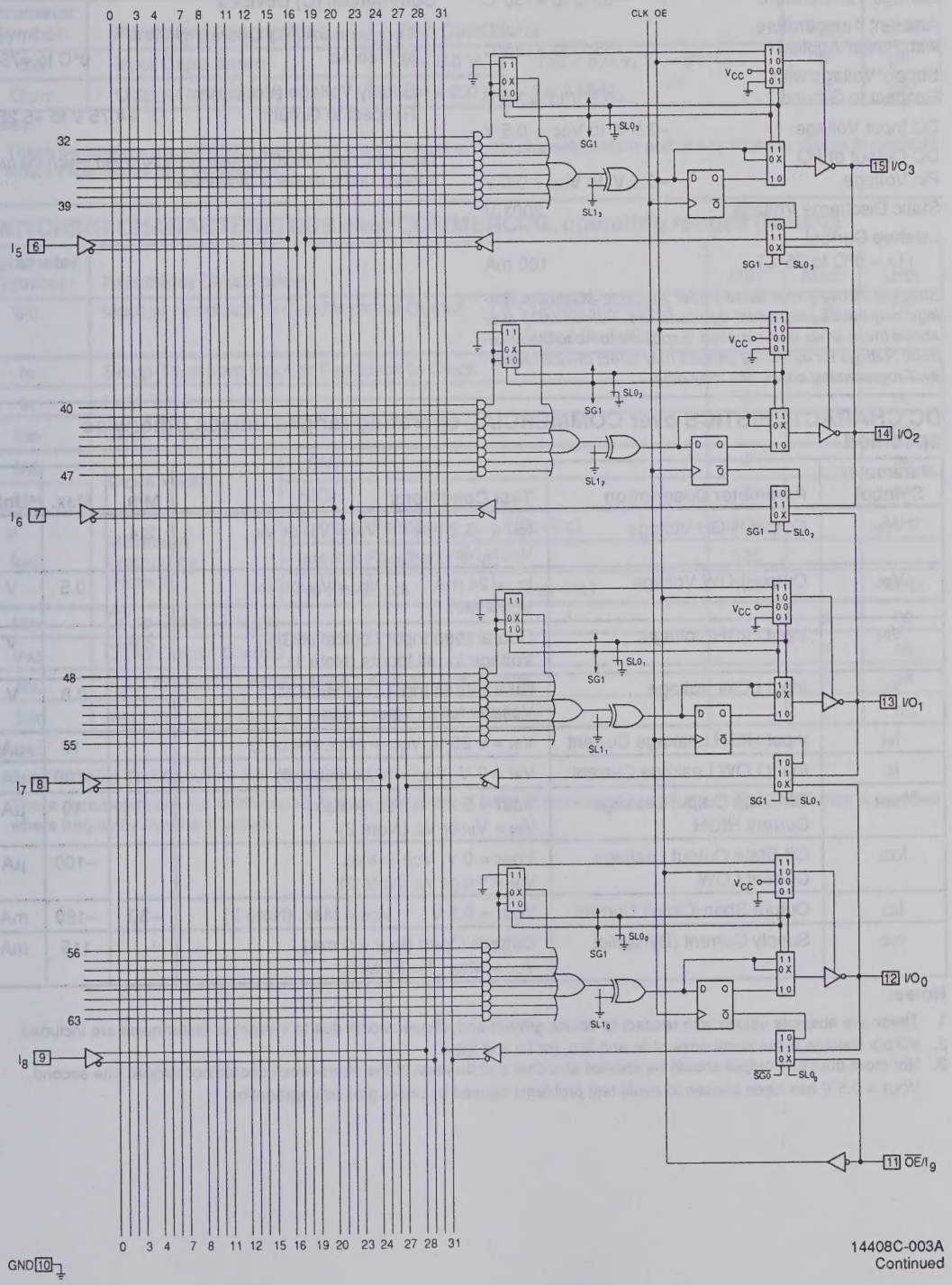
Technology

The high-speed PALCE16V8 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



LOGIC DIAGRAM (Continued)



14408C-003A
Continued

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max. (Note 3)	−30	−150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz		115	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output		8 Outputs Switching		7.5	ns
			1 Output Switching		7	ns
t_S	Setup Time from Input or Feedback to Clock			5		
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				5	ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	100		MHz
		Internal Feedback (f_{CNT})		125		
		No Feedback	$1/(t_{WH}+t_{WL})$	125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				6	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				6	ns
t_{EA}	Input to Output Enable Using Product Term Control				9	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max. (Note 3)	−30	−150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz		115	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})		71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				10	ns
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

0ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max. (Note 3)		−30	−150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz	H		90	mA
			Q		55	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{WL}	Clock Width	LOW		8		12		ns
t_{WH}		HIGH		8		12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	45.5		37		MHz
		Internal Feedback (f_{CNT})		50		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		20	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		20	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 1.0 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 1.0 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = −55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	−55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.0 V, V_{OUT} = 0.5 V (Note 5), T = 25°C	−30	−150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz		130	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input or Feedback to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				7	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	58.5		MHz
		Internal Feedback (f_{CNT})		62.5		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				10	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				10	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				10	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 1.0 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 1.0 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = −55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	−55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.0 V, V_{OUT} = 0.5 V (Note 5), T = 25°C	−30	−150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz		130	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input or Feedback to Clock			12		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				12	ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	41.6		MHz
		Internal Feedback (f_{CNT})		45.5		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				15	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 1.0 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 1.0 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = −55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	−55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.0 V, V_{OUT} = 0.5 V (Note 5), T = 25°C	−30	−150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz		130	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

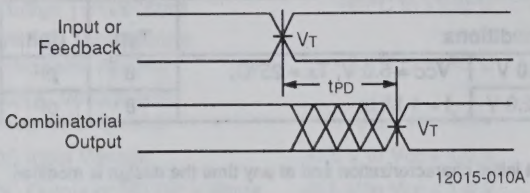
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20		25	ns
t_S	Setup Time from Input or Feedback to Clock			15		15		
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				15		20	ns
t_{WL}	Clock Width	LOW		12		15		ns
t_{WH}		HIGH		12		15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	33.3		28.6		MHz
		Internal Feedback (f_{CNT})		35.7		30.3		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	41.7		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				20		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				20		20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				20		55	ns

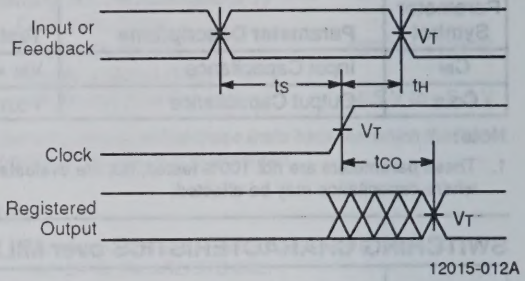
Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

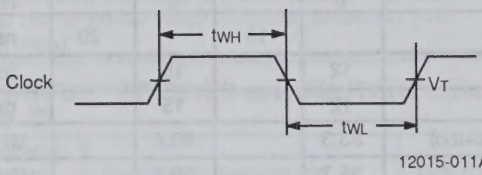
SWITCHING WAVEFORMS



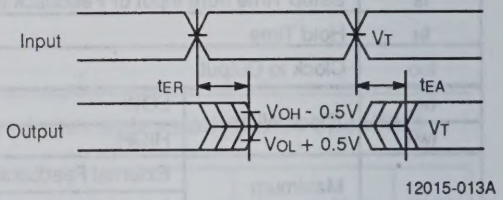
Combinatorial Output



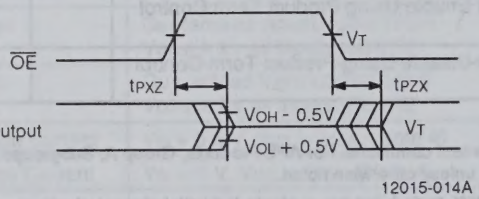
Registered Output



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

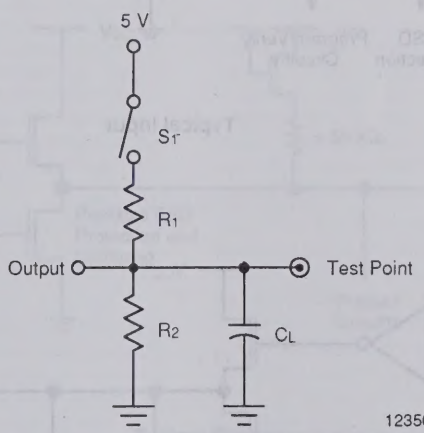
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12350-019A

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

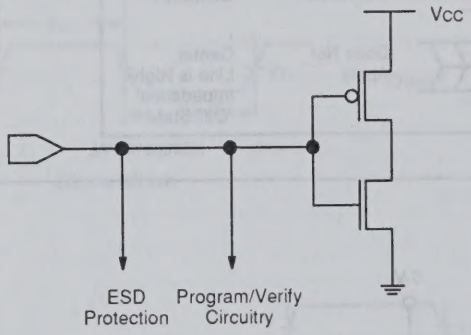
ENDURANCE CHARACTERISTICS

The PALCE16V8 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

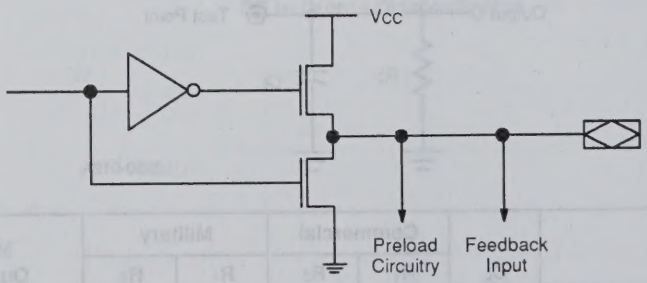
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



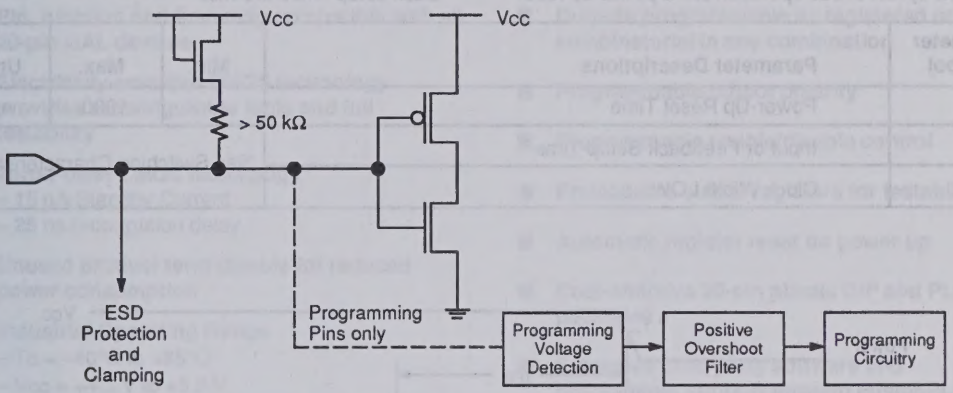
Typical Output

12197-013A

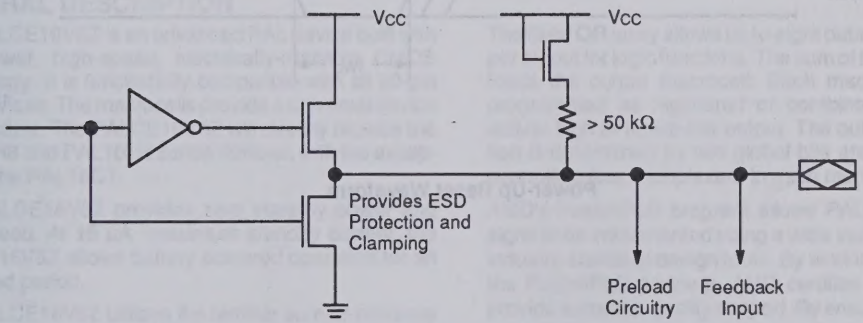
ROBUSTNESS FEATURES FOR /5 VERSIONS

The PALCE16V8H-7/5 has some unique features that make it extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSION



Typical Input



Typical Output

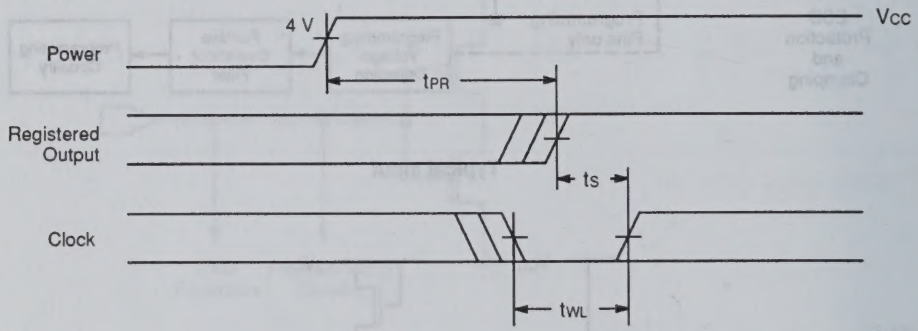
16407A-001B

POWER-UP RESET

The PALCE16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways Vcc can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The Vcc rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		1000	ns
ts	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



12350-024A

Power-Up Reset Waveform

PALCE16V8Z-25

Zero-Power 20-Pin EE CMOS Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Pin, function and fuse-map compatible with all 20-pin GAL devices
- Electrically-erasable CMOS technology provides reconfigurable logic and full testability
- Zero-Power CMOS technology
  - 15 µA Standby Current
  - 25 ns propagation delay
- Unused product term disable for reduced power consumption
- Industrial Operating Range
  - T_C = –40°C to +85°C
  - V_{CC} = +4.5 V to +5.5 V
- HC- and HCT-Compatible inputs and outputs
- Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series
- Outputs programmable as registered or combinatorial in any combination
- Programmable output polarity
- Programmable enable/disable control
- Preloadable output registers for testability
- Automatic register reset on power up
- Cost-effective 20-pin plastic DIP and PLCC packages
- Extensive third-party software and programmer support through FusionPLD partners
- Fully tested for 100% programming and functional yields and high reliability

GENERAL DESCRIPTION

The PALCE16V8Z is an advanced PAL device built with zero-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8Z will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

The PALCE16V8Z provides zero standby power and high speed. At 15 µA maximum standby current, the PALCE16V8Z allows battery powered operation for an extended period.

The PALCE16V8Z utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active- high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE16V8Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

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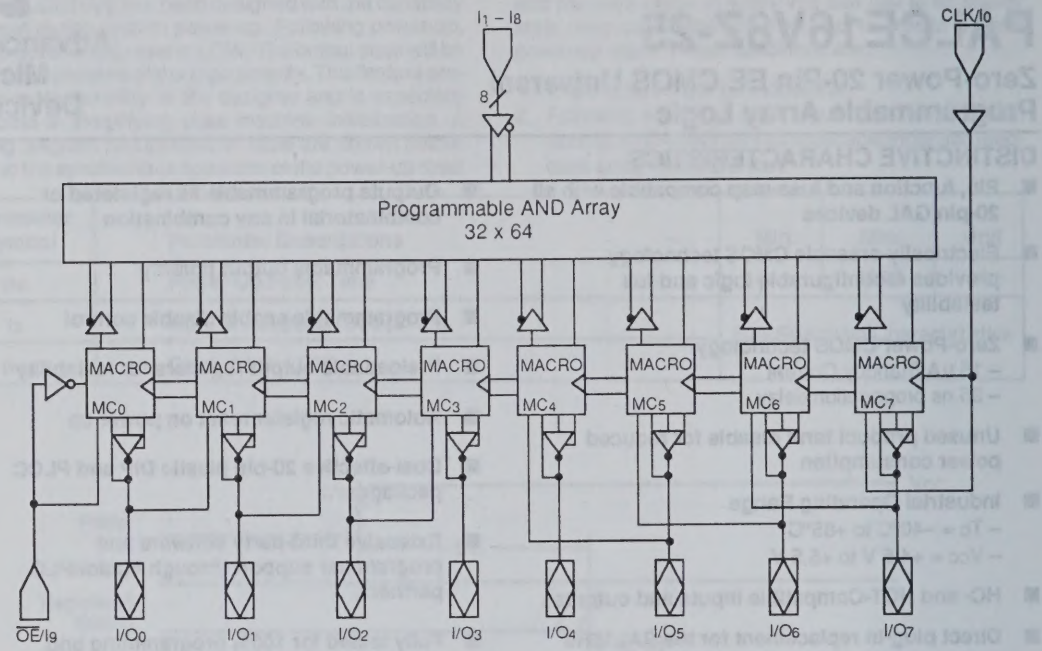
Issue Date: January 1992

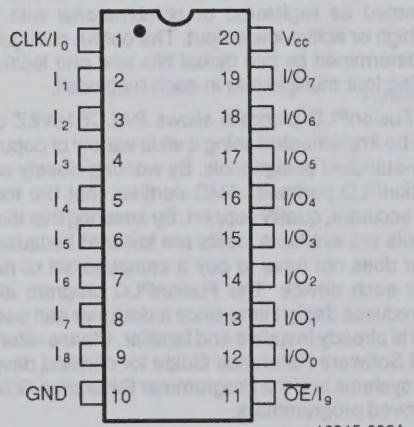
BLOCK DIAGRAM



12197-001B

CONNECTION DIAGRAMS
Top View

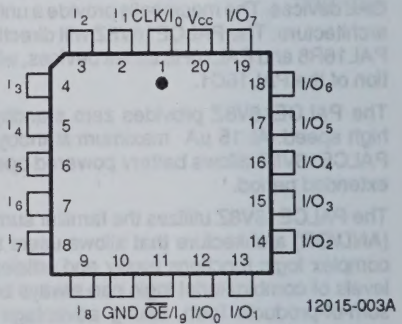
DIP



12015-002A

Note: Pin 1 is marked for orientation

PLCC/LCC



12015-003A

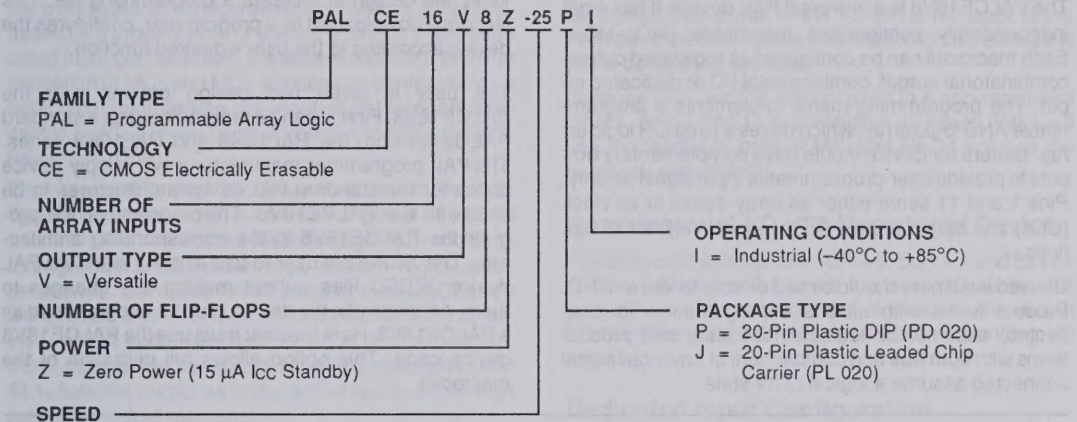
PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
$\overline{OE}$	=	Output Enable
Vcc	=	Supply Voltage

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE16V8Z-25	PI, JI

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

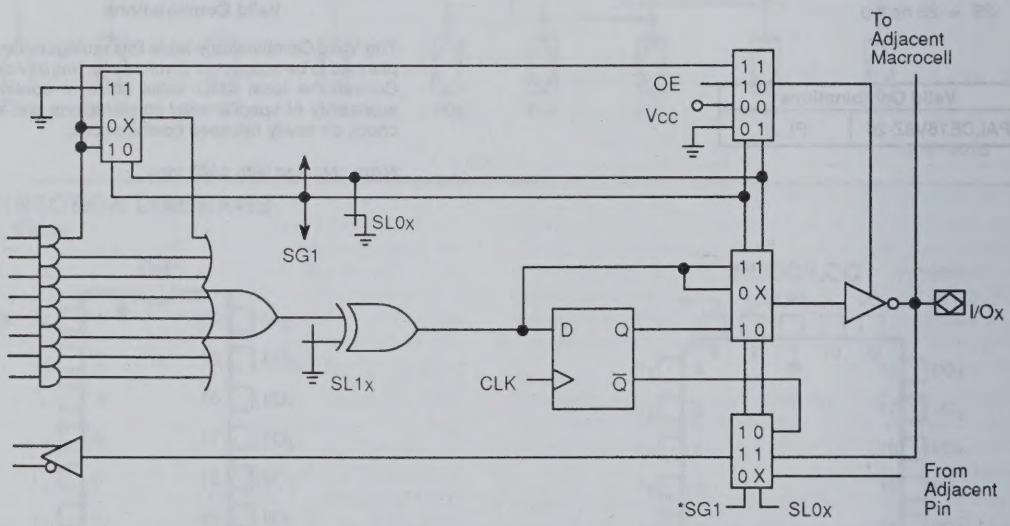
The PALCE16V8Z is the zero-power version of the PALCE16V8. It has all the architectural features of the PALCE16V8. In addition, the PALCE16V8Z has zero standby power and unused product term disable.

The PALCE16V8 is a universal PAL device. It has eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8. The programmer will program the PALCE16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8. Here the user must use the PALCE16V8 device code. This option allows full utilization of the macrocell.



*In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.

12197-004A

PALCE16V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 11 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8 will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of MC_3 and MC_4. MC_3 and MC_4 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 11 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

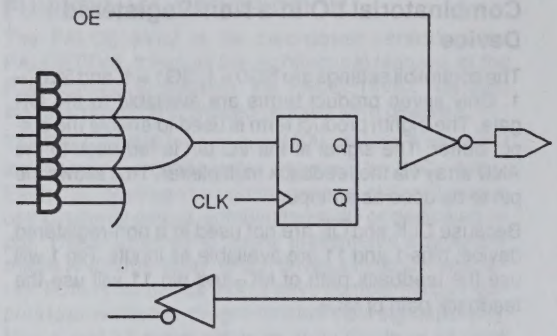
Table 1. Macrocell Configuration

SG0	SG1	SL0x	Cell Configuration	Devices Emulated
Device Uses Registers				
0	1	0	Registered Output	PAL16R8, 16R6, 16R4
0	1	1	Combinatorial I/O	PAL16R6, 16R4
Device Uses No Registers				
1	0	0	Combinatorial Output	PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2
1	0	1	Input	PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2
1	1	1	Combinatorial I/O	PAL16L8

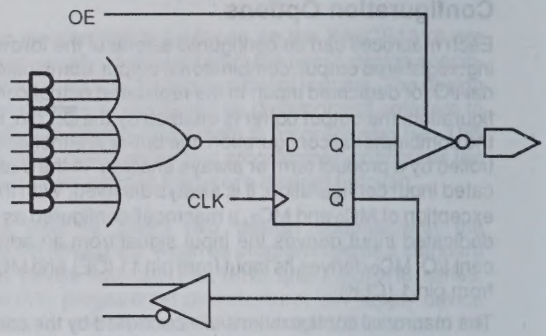
Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

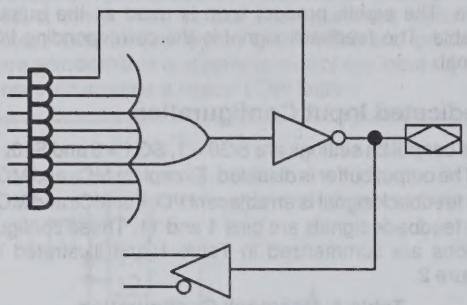
Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



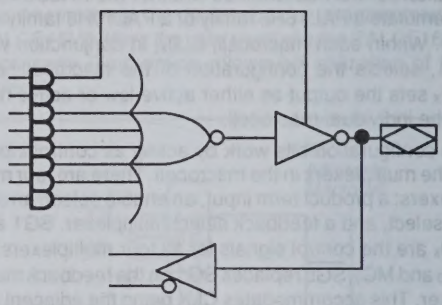
Registered Active Low



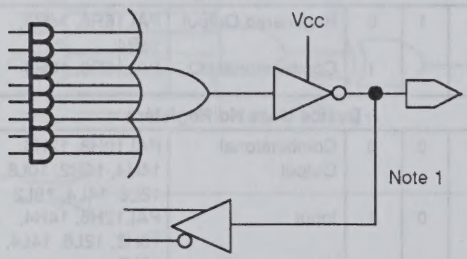
Registered Active High



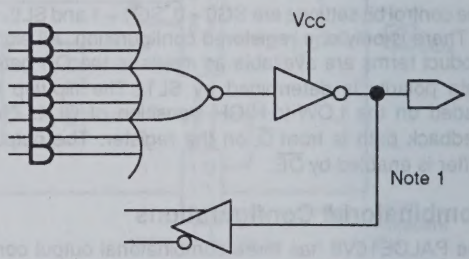
Combinatorial I/O Active Low



Combinatorial I/O Active High



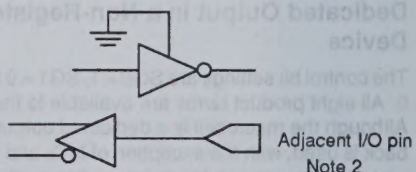
Combinatorial Output Active Low



Combinatorial Output Active High

Notes:

1. Feedback is not available on pins 15 and 16 in the combinatorial output mode.
2. The dedicated-input configuration is not available on pins 15 and 16.



Dedicated Input

12197-012B

Figure 2. Macrocell Configurations

Zero-Standby Power Mode

The PALCE16V8Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE16V8Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero ($I_{CC} < 15\ \mu A$). The outputs will maintain the states held before the device went into the standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the I_{CC} vs. frequency graph.

Product-Term Disable

On a programmed PALCE16V8Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the I_{CC} vs frequency graphs, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

The preload function is not disabled by the security bit. This allows functional testing after the security bit is programmed.

Security Bit

A security bit is provided on the PALCE16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its unprogrammed state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

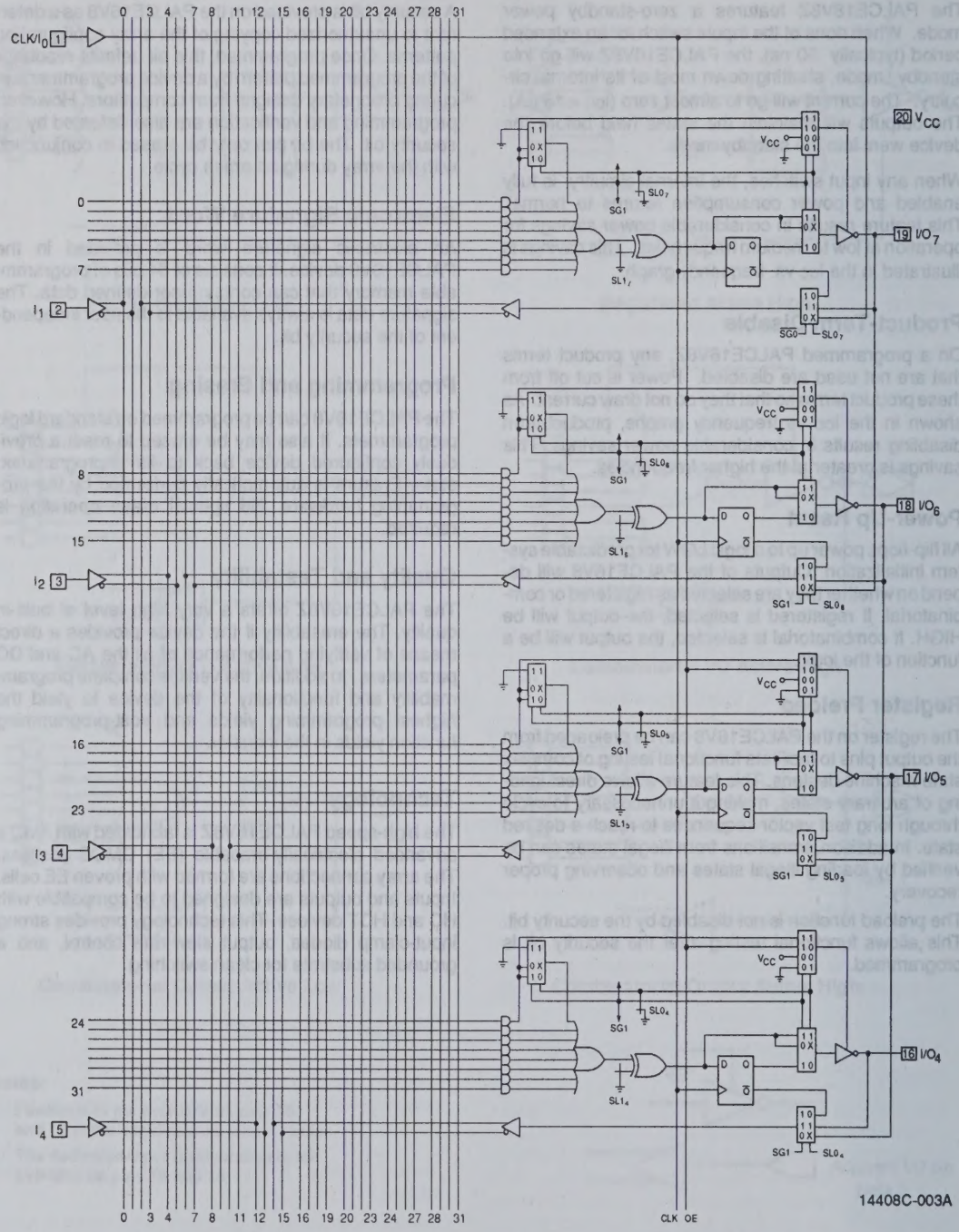
Quality and Testability

The PALCE16V8Z offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, the verifies complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

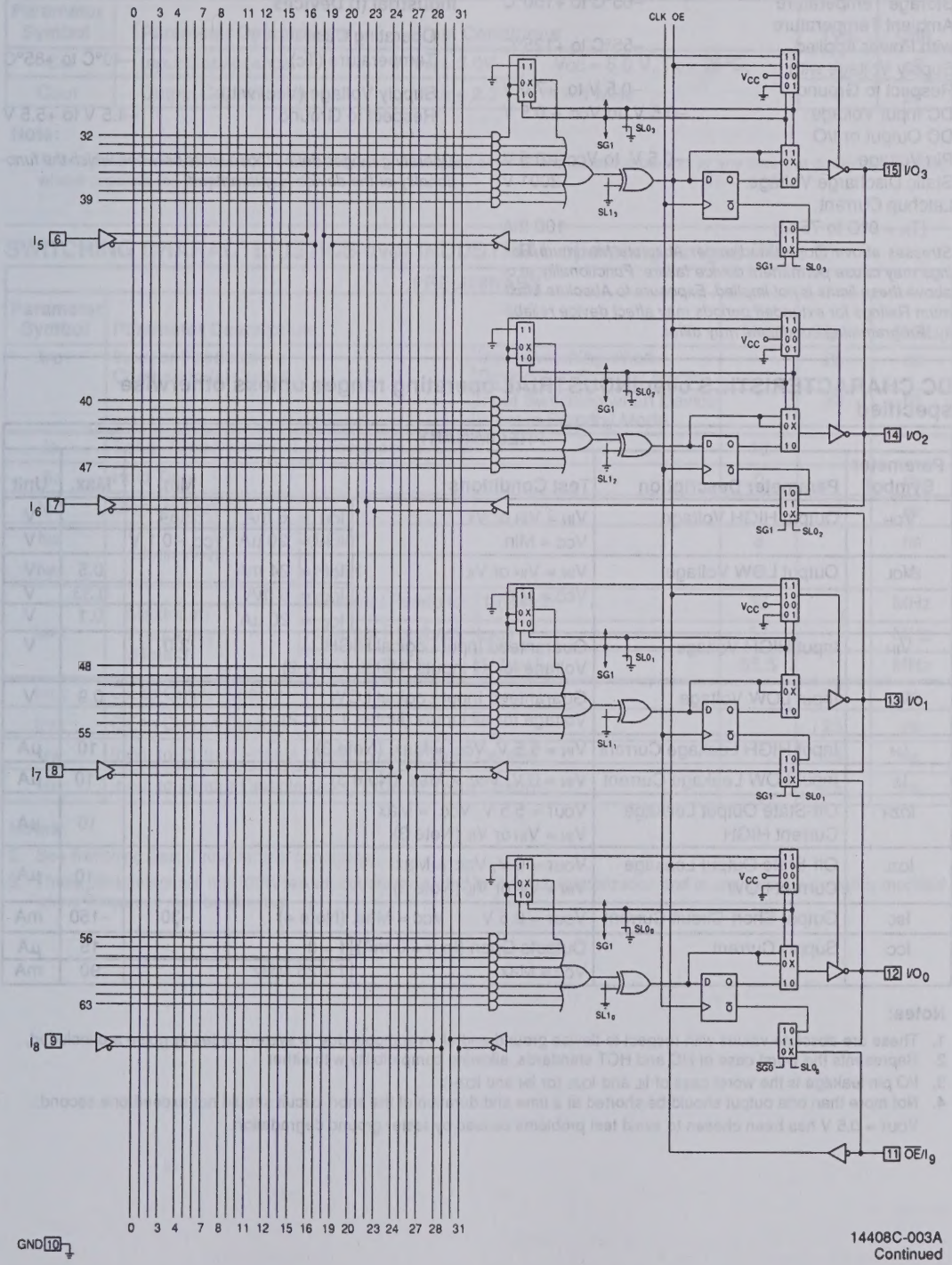
Technology

The high-speed PALCE16V8Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



LOGIC DIAGRAM (Continued)



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Continued

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case Temperature (T_C)	−40°C to +85°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 6 mA	3.84		V
		V_{CC} = Min.	I_{OH} = 20 µA	V_{CC} − 0.1 V		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.5	V
		V_{CC} = Min.	I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1 and 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1 and 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 3)			−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)			−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max. (Note 4)		−30	−150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0		15	µA
		V_{CC} = Max.	f = 25 MHz		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Represents the worst case of HC and HCT standards, allowing compatibility with either.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

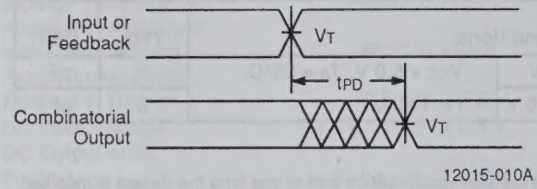
PRELIMINARY

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output		Input Switching when Device is in Standby Mode		25	ns
			Input Switching when Device is not in Standby Mode		23	ns
t_S	Setup Time from Input or Feedback to Clock			18		
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				12	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	33		MHz
		Internal Feedback (f_{CNT})		50		MHz
		No Feedback	$1/(t_{SU}+t_H)$	55.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				25	ns
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

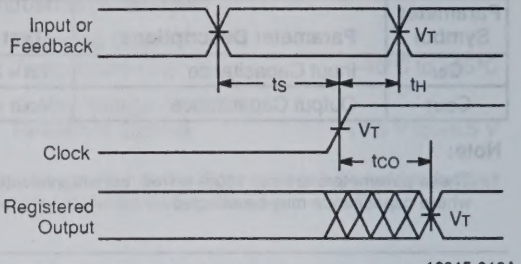
Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

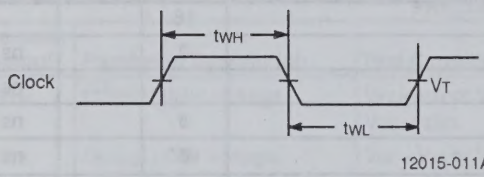
SWITCHING WAVEFORMS



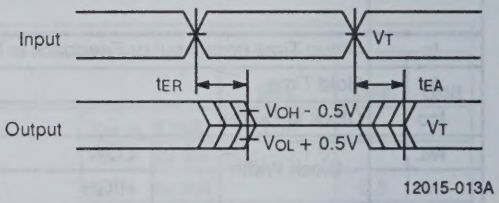
Combinatorial Output



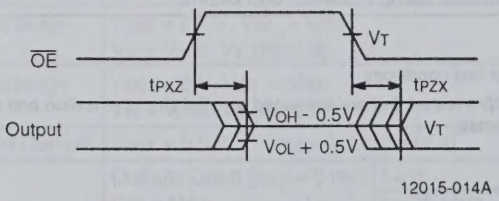
Registered Output



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V for Input Signals and 2.5 V for Output Signals.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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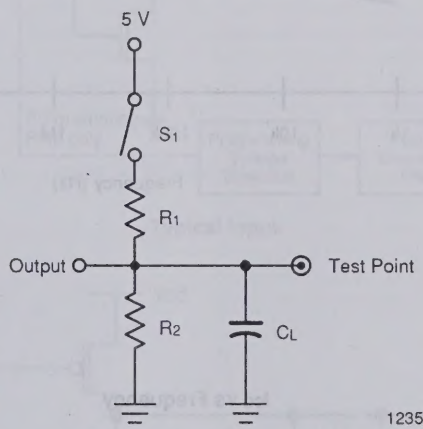
SWITCHING TEST CIRCUIT



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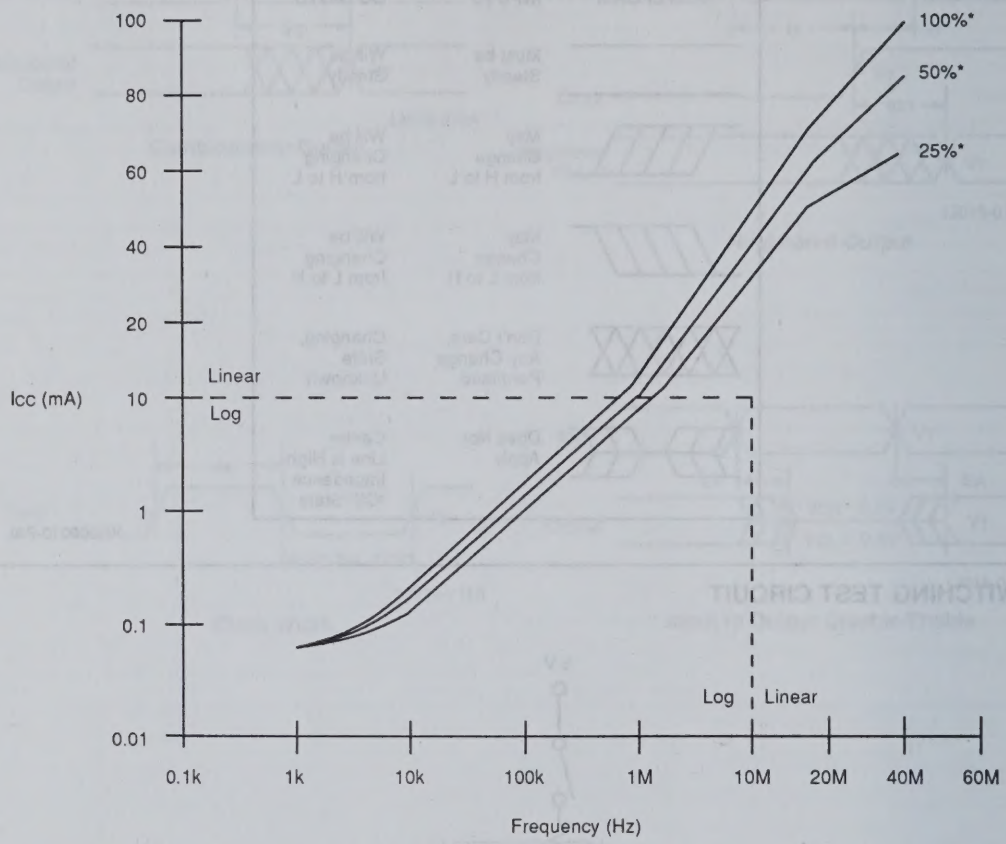
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	30 pF	820 Ω	820 Ω	2.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				2.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



15700A-002B

*Percent of product terms used.

I_{CC} vs Frequency

ENDURANCE CHARACTERISTICS

The PALCE16V8Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

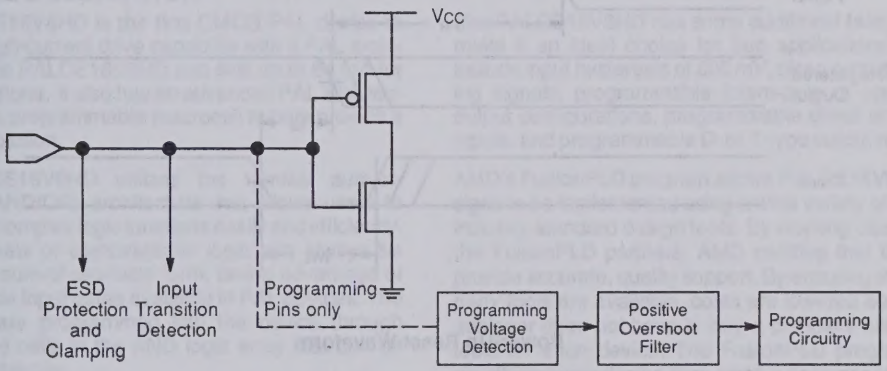
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	20	Years	Max. Operating Temperature
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

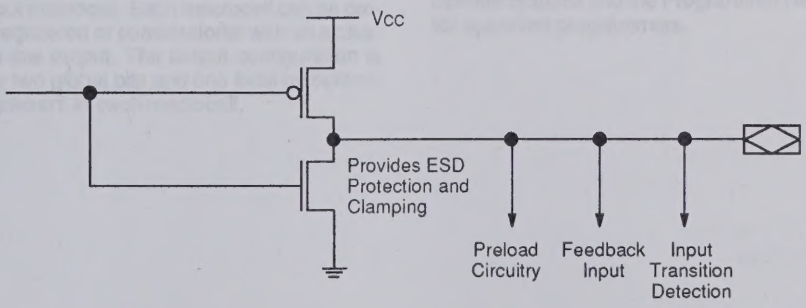
ROBUSTNESS FEATURES

The PALCE16V8Z-25 has some unique features that make it extremely robust, especially when operating in high-speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

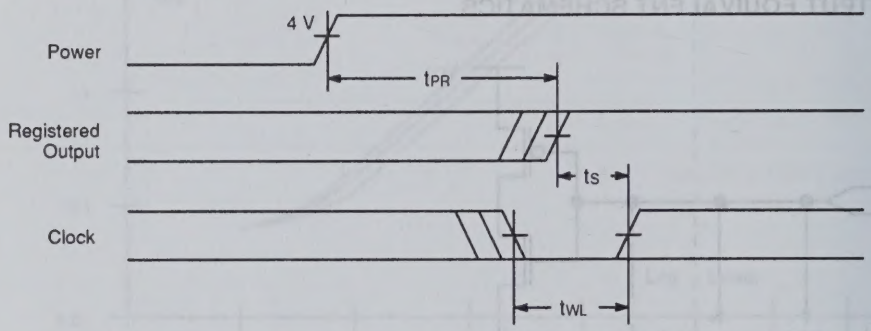
13061B-003A

POWER-UP RESET

The PALCE16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways Vcc can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The Vcc rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		1000	ns
ts	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



12350-024A

Power-Up Reset Waveform

COM'L

PALCE16V8HD-15

EE CMOS 24-Pin High-Drive Universal PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- High output-current drive capability (64 mA I_{OL})
- Programmable Totem-Pole or Open-Drain Outputs
- 200 mV Hysteresis
- Programmable Direct or Latched Inputs
- Outputs configurable as D or T flip-flops
- Outputs programmable as registered or combinatorial in any combination
- Automatic register reset on power-up
- Preloadable output registers for testability
- Programmable enable/disable control
- Electrically Erasable CMOS technology provides reconfigurable logic and full testability
- Cost-effective 24-pin plastic SKINNYDIP® and 28-pin PLCC packages
- Extensive third-party software and programmer support through FusionPLD partners
- Fully tested for 100% programming and functional yields and high reliability

GENERAL DESCRIPTION

The PALCE16V8HD is the first CMOS PAL device to combine high-current drive capability with a PAL architecture. The PALCE16V8HD can sink up to 64 mA for bus applications. It also has an advanced PAL architecture using a programmable macrocell to help provide a universal solution.

The PALCE16V8HD utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

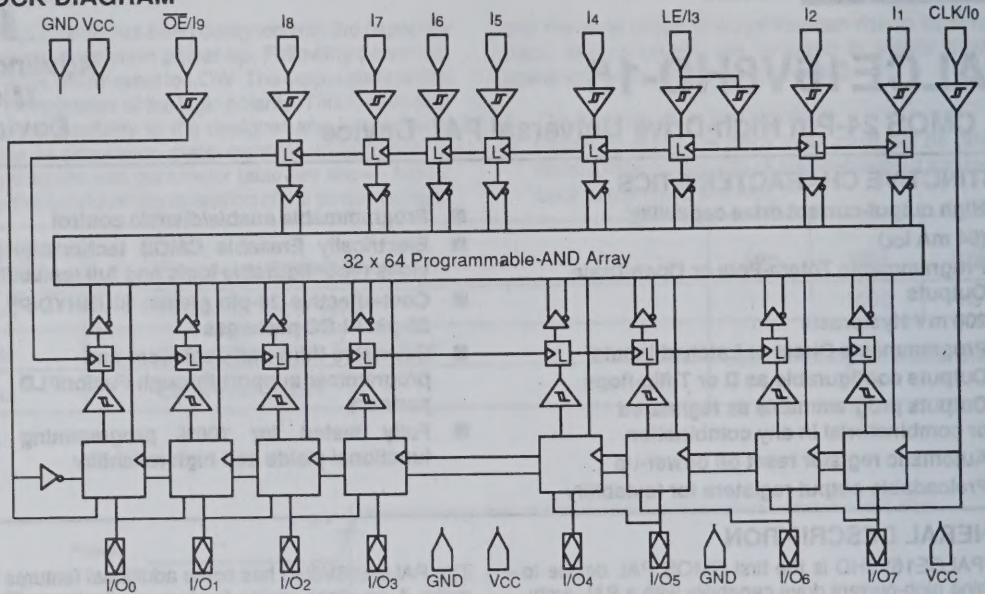
The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

The PALCE16V8HD has some additional features that make it an ideal choice for bus applications. These include input hysteresis of 200 mV, clean output-switching signals, programmable totem-pole or open-drain output configurations, programmable direct or latched inputs, and programmable D- or T-type output registers.

AMD's FusionPLD program allows PALCE16V8HD designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 15559 Rev. C Amendment/0
Issue Date: January 1992

BLOCK DIAGRAM

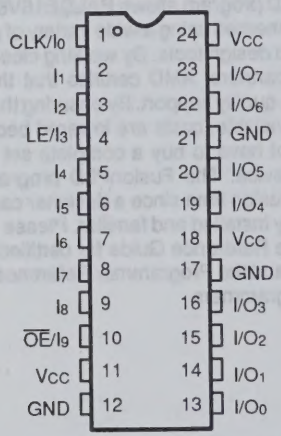


15559B-001B

CONNECTION DIAGRAMS

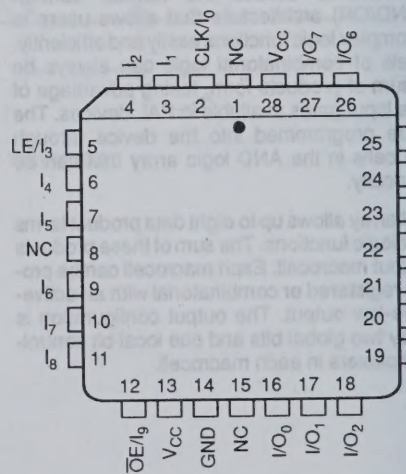
Top View

SKINNYDIP



15559-002A

PLCC/LCC



15559-003A

Note:

Pin 1 is marked for orientation.

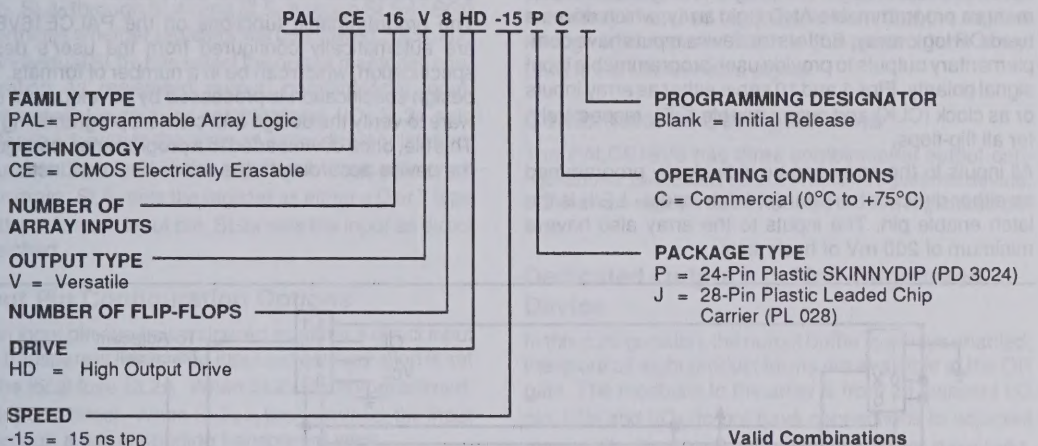
PIN DESIGNATIONS

CLK = Clock
LE = Latch Enable
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
$\overline{OE}$ = Output Enable
VCC = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE16V8HD-15	PC, JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

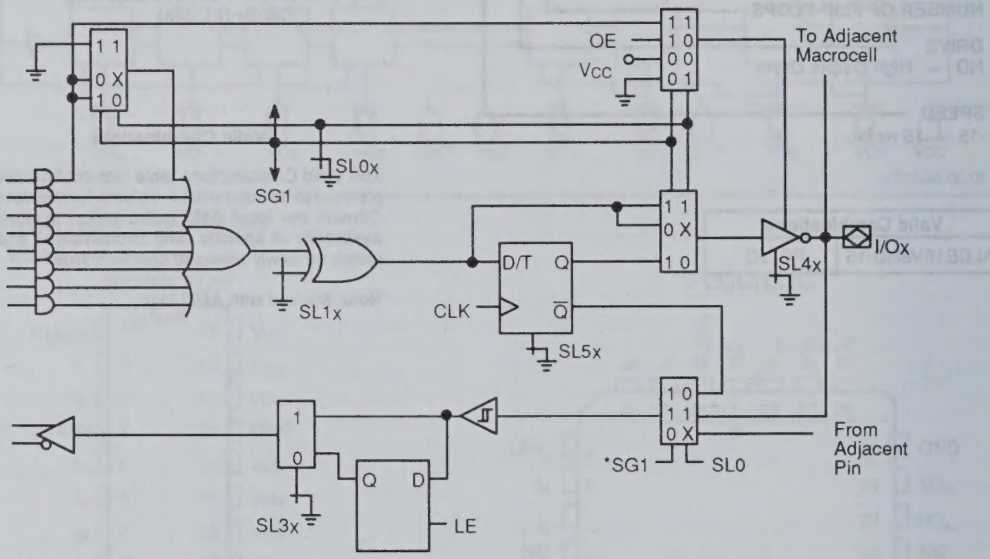
FUNCTIONAL DESCRIPTION

The PALCE16V8HD is a universal PAL device with eight independently configurable macrocells (MC_0–MC_7). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 10 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

All inputs to the array can be individually programmed as either direct or transparent-latch inputs. LE/I_3 is the latch enable pin. The inputs to the array also have a minimum of 200 mV of hysteresis.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8HD are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.



*In macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.

15559-004A

Figure 1. PALCE16V8HD I/O Macrocell

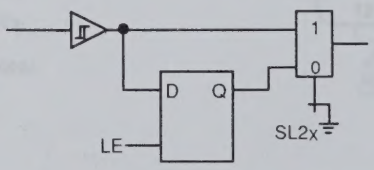


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Figure 2. PALCE16V8HD Input Macrocell

Device Configuration

The configuration of the PALCE16V8HD is controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 48 local bits ($SL0_0$ through $SL0_7$, $SL1_0$ through $SL1_7$, $SL2_1$ through $SL2_8$, $SL3_0$ through $SL3_7$, $SL4_0$ through $SL4_7$ and $SL5_0$ through $SL5_7$). SG0 determines whether registers will be allowed. SG1 and the individual SL0x bits select the output macrocell configuration as registered output, combinatorial input, combinatorial output, or combinatorial I/O. SL3x sets the feedback path to the array as either direct or latched. SL4x sets the output buffer as either a totem pole or an open drain. SL5x sets the register as either a D or T type flip-flop. At each input pin, SL2x sets the input as direct or latched.

Input Pin Configuration Options

Each input pin can be configured as either a direct input or a transparent latch. The input-pin configuration is set by the local fuse SL2x. When SL2x is unprogrammed, the input is direct. When SL2x is programmed, the input is through a corresponding transparent latch.

The latch is enabled via LE/I_3. The latches hold data when LE/I_3 is low. They are transparent when LE/I_3 is HIGH.

I/O Macrocell Configuration Options

Each I/O macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 10 ($\overline{OE}$) and MC_7 from pin 1 (CLK). These configurations are summarized in Table 1 and illustrated in Figure 3.

The feedback path in each macrocell can be programmed as either direct or latched. The feedback configuration is set by the local fuse SL3x. When SL3x is unprogrammed, the corresponding feedback path is direct to the array. When SL3x is programmed, the corresponding feedback path is through a corresponding transparent latch.

The latch is enabled via LE/I_3. The latches hold data when LE/I_3 is LOW. They are transparent when LE/I_3 is HIGH.

Registered Output Configurations

There are two registered configurations: D type and T type. The type is selected by SL5x.

In the registered configurations all eight product terms are available as inputs to the OR gate. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The output buffer is enabled by OE.

Feedback to the array can be either direct or latched. Direct feedback is from Q of the register to the product-term array. Latched feedback is from Q of the register through a transparent latch to the product-term array. LE/I_3 is the latch-enable signal.

Combinatorial Configurations

The PALCE16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

In this configuration, the output buffer is always enabled; therefore all eight product terms are available to the OR gate. The feedback to the array is from an adjacent I/O pin. I/O_3 and I/O_4 do not have connections to adjacent macrocells; therefore, MC_3 and MC_4 do not have feedback to the array in this mode.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 10 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 10 will use the feedback path of MC_0.

Combinatorial I/O In a Non-Registered Device

Only seven product terms are available to the OR gate in this configuration. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 10 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 10 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

In this configuration only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Dedicated Input Configuration

The output buffer is disabled in this configuration. Except for MC_0 and MC_7 the feedback signal is an adjacent I/O. For MC_0 and MC_7 the feedback signals are pins 1 and 10.

Pins 16 (19) and 19 (23) do not have connections to adjacent macrocells. The dedicated-input configuration is not available on these pins.

Table 1. Macrocell Configuration

SG0	SG1	$SL0_X$	$SL0_5$	Cell Configuration
Device Uses Registers				
0	1	0	0	T-Type Registered Output
0	1	0	1	D-Type Registered Output
Device Uses No Registers				
1	0	0	X	Combinatorial Output
1	0	1	X	Dedicated Input
1	1	1	X	Combinatorial I/O

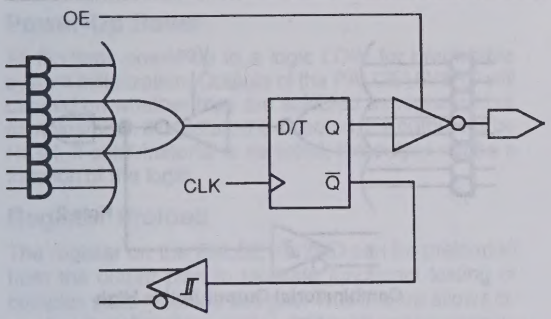
Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

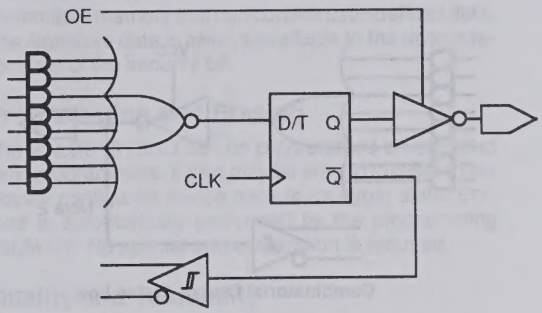
Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.

Output Buffer Configurations

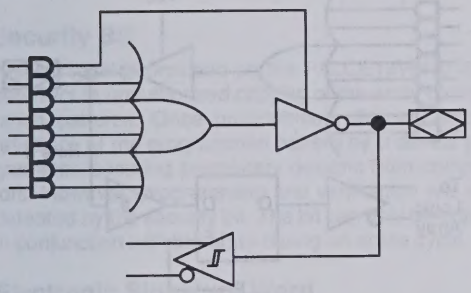
The output buffer can be configured as either a totem-pole output or an open-drain output. This configuration is set by $SL4_x$. The buffer is a totem-pole output when $SL4_x$ is unprogrammed and an open-drain output when $SL4_x$ is programmed. In the totem-pole configuration, the output voltage levels are the standard V_{OH} and V_{OL} levels. In the open-drain configuration, V_{OL} is the standard value. However, V_{OH} will depend on the termination circuitry.



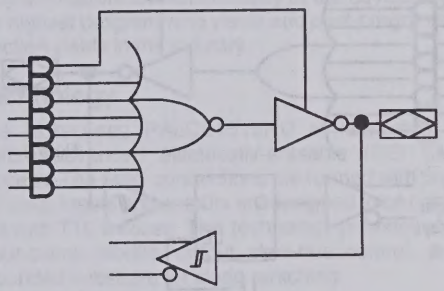
Registered Active Low



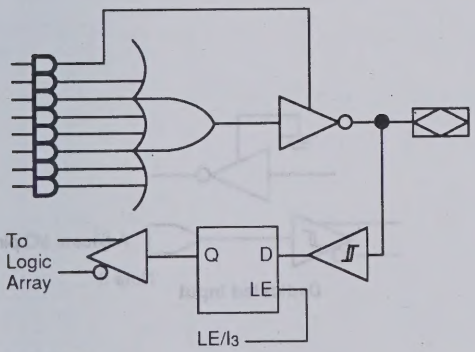
Registered Active High



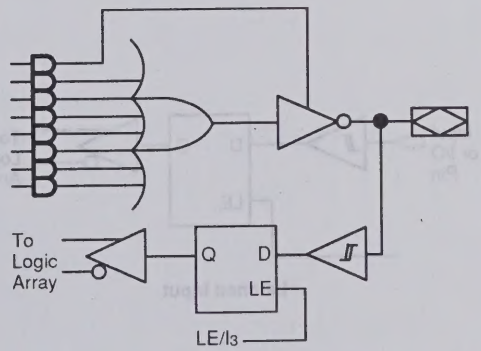
Combinatorial I/O Active Low



Combinatorial I/O Active High



Combinatorial I/O Active Low
with Latched Feedback



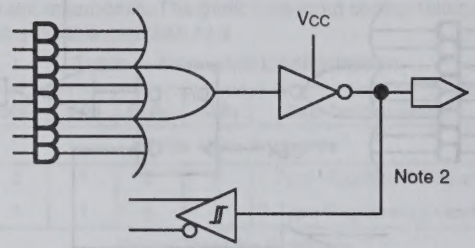
Combinatorial I/O Active High
with Latched Feedback

Note:

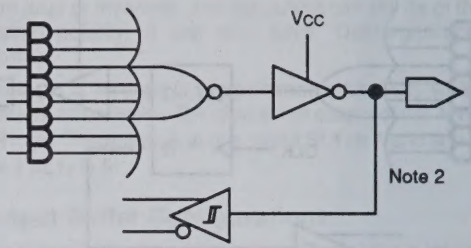
1. All output and I/O configurations are valid as either totem-pole outputs or open-collector outputs.

15559B-006B

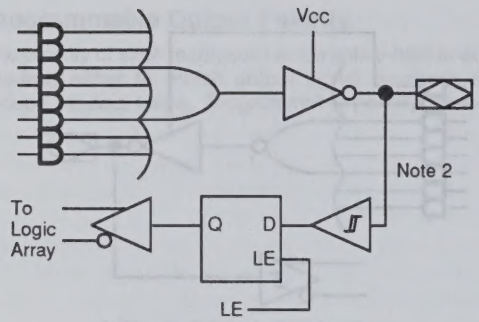
Figure 3. Macrocell Configurations



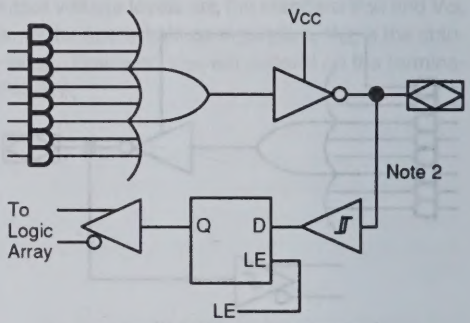
Combinatorial Output Active Low



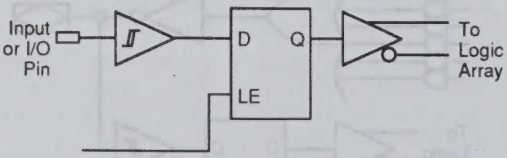
Combinatorial Output Active High



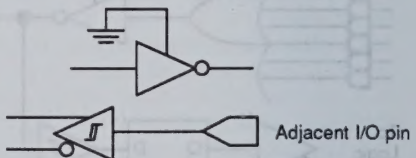
Combinatorial Output Active Low
with Latched Feedback



Combinatorial Output Active High
with Latched Feedback



Latched Input



Dedicated Input

15559B-007B

Notes:

1. All output and I/O configurations are valid as either totem-pole outputs or open-collector outputs.
2. Feedback is not available on pins 16 and 19 in the combinatorial output mode.
3. The dedicated-input configuration is not available on pins 16 and 19.

Figure 4. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8HD will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE16V8HD can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE16V8HD as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE16V8HD device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE16V8HD can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

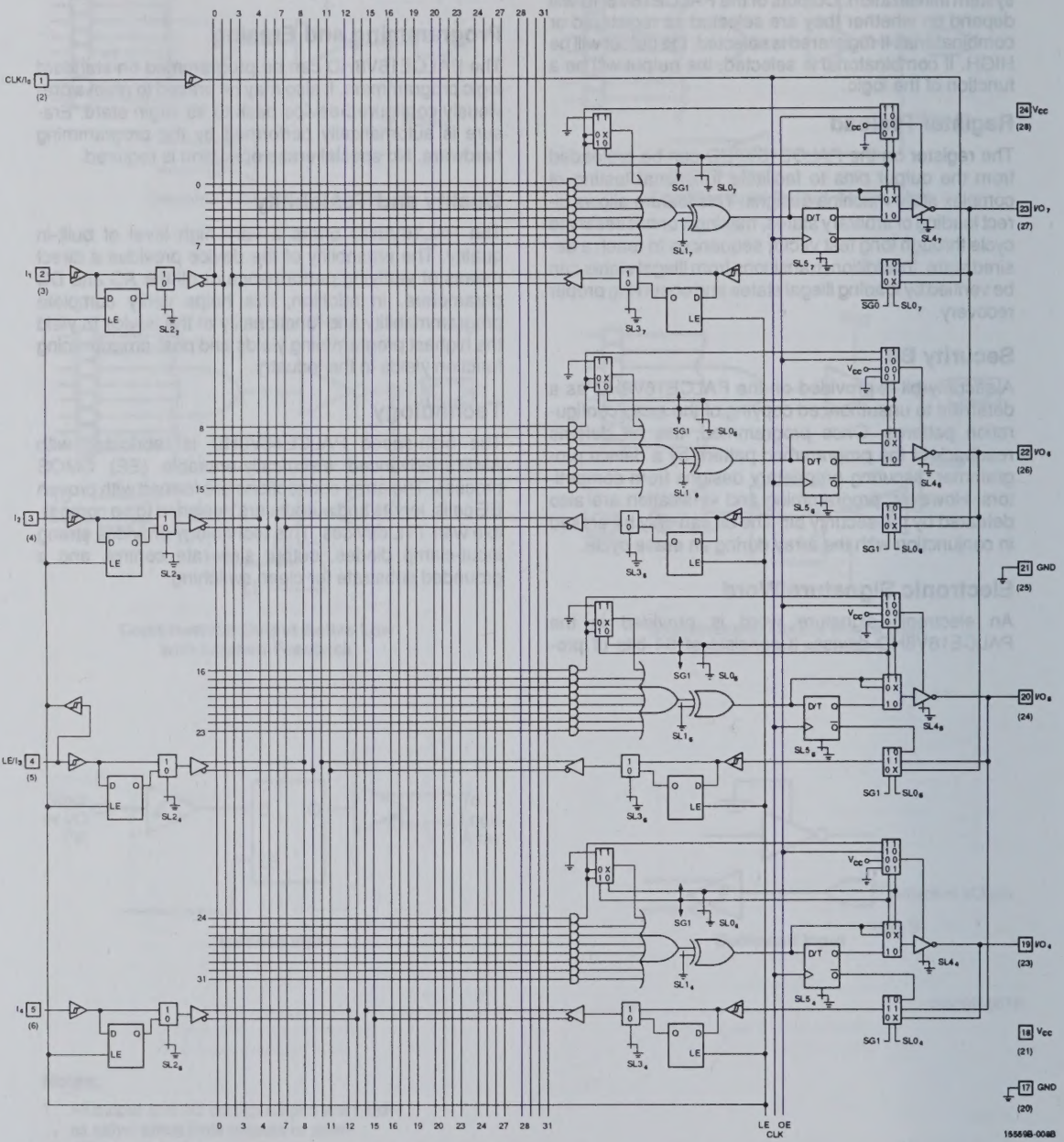
Quality and Testability

The PAL16V8HD offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this helps verify complete programmability and functionality of the device to yield the highest programming yields and post-programming function yields in the industry.

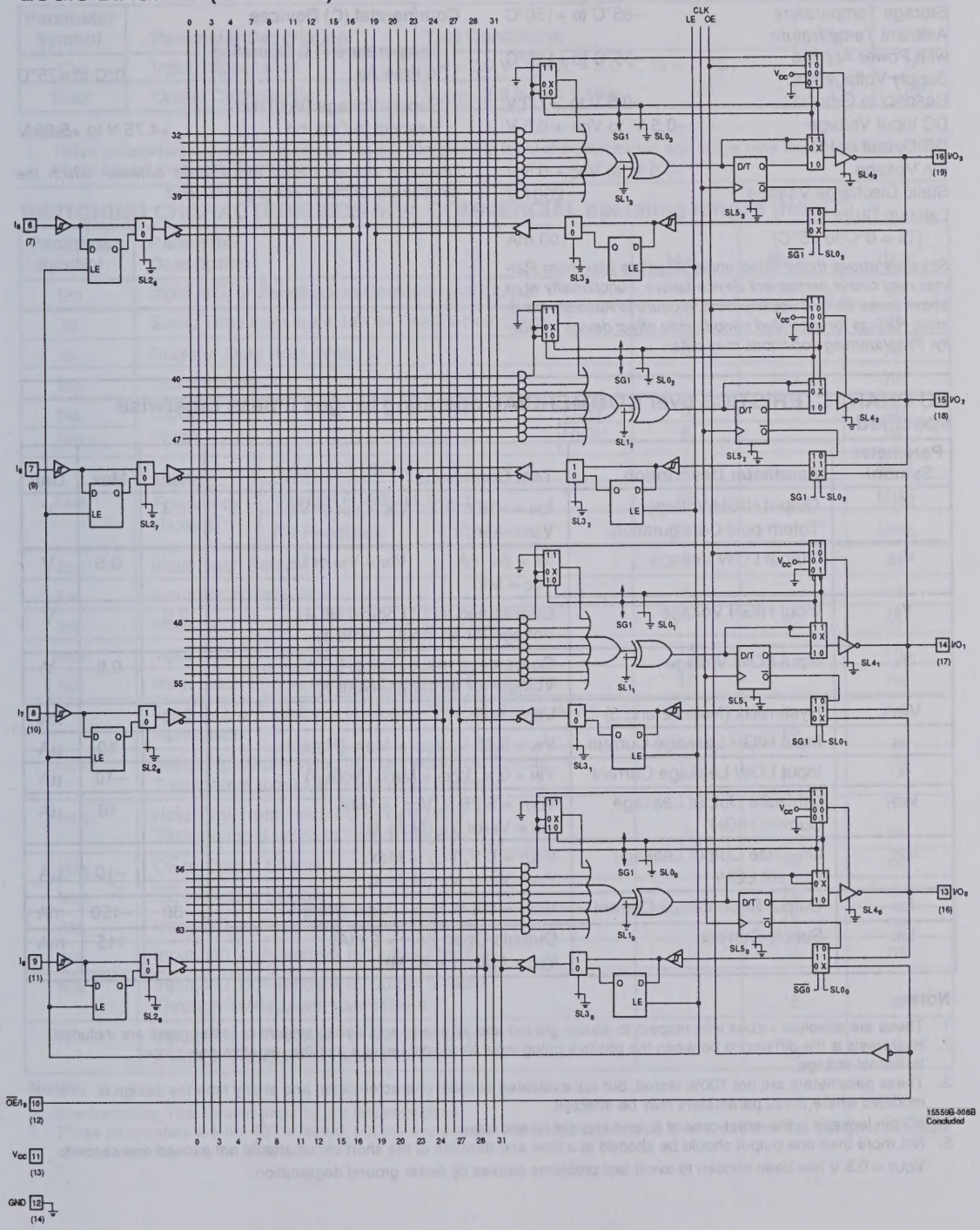
Technology

The high-speed PALCE16V8HD is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP/Flatpack (PLCC/LCC) Pinouts



LOGIC DIAGRAM (Continued)



ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage Totem-pole Configuration	I_{OH} = –16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 64 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_{HYS}	Hysteresis (Notes 2 and 3)	V_{CC} = Min.	200		mV
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz		115	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Hysteresis is the difference between the positive going input threshold voltage and the negative going input threshold voltage.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

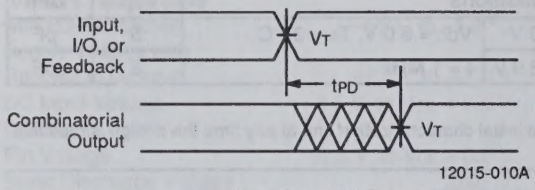
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			10		ns
t_H	Register Data Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width		LOW	6		ns
t_{WH}			HIGH	6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})		66		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$	83.3		MHz
t_{SIL}	Input Latch Setup Time			4		ns
t_{HIL}	Input Latch Hold Time			6		ns
t_{IGO}	Input Latch Enable to Combinatorial Output				15	ns
t_{WIGH}	Input Latch Enable Width HIGH			15		ns
t_{IGS}	Input Latch Enable to Output Register Setup Time			10		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch				15	ns
t_{SLR}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Register			10		ns
t_{HLR}	Hold Time from Input, I/O or Feedback Through Input Latch to Output Register			0		ns
t_{PZX}	$\overline{OE}$ to Output Enable				15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15	ns
t_{EA}	Input, I/O, or Feedback to Output Enable				15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable				15	ns
t_{EAL}	Input, I/O, or Feedback to Output Enable Through Transparent Latch (Note 3)				15	ns
t_{ERL}	Input, I/O, or Feedback to Output Disable Through Transparent Latch (Note 3)				15	ns

Notes:

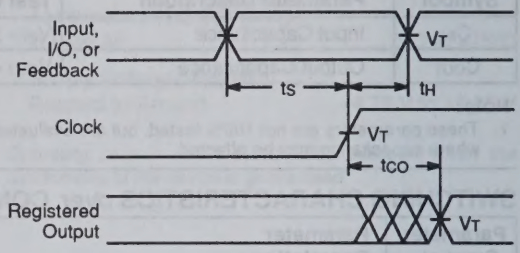
2. See Switching Test Circuit, page 15, for test conditions.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



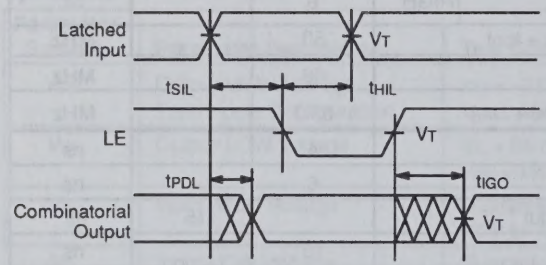
12015-010A

Combinatorial Output



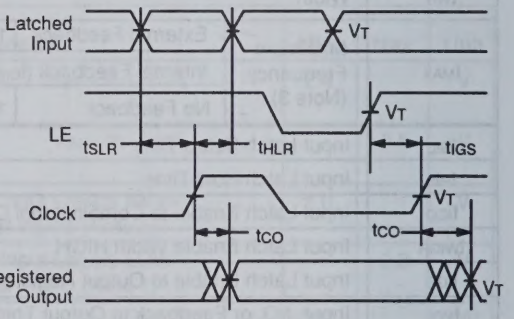
15559-009A

Registered Output



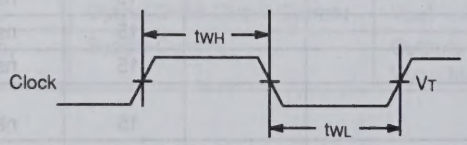
15559-011A

Latched Input with Combinatorial Output



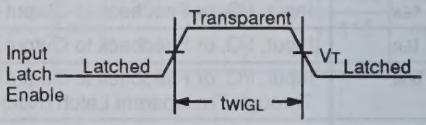
15559B-010B

Latched Input with Registered Output



15559B-015A

Clock Width



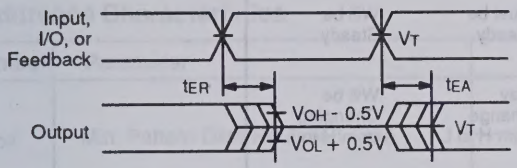
15559B-012B

Input Latch Enable Width

Notes:

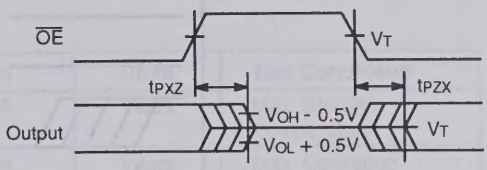
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

SWITCHING WAVEFORMS



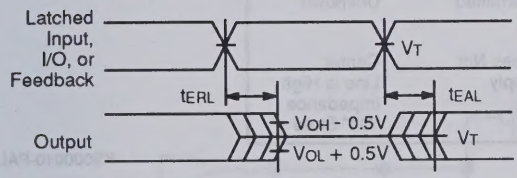
10232-008A

Input to Output Disable/Enable



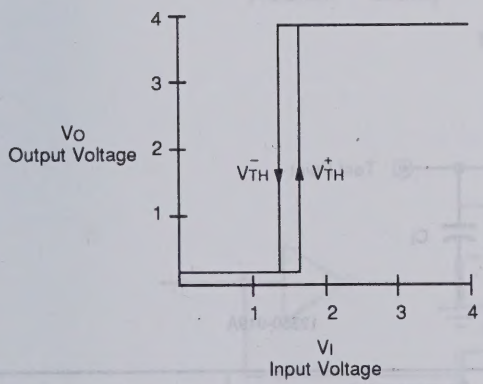
12015-014A

$\overline{OE}$ to Output Disable/Enable

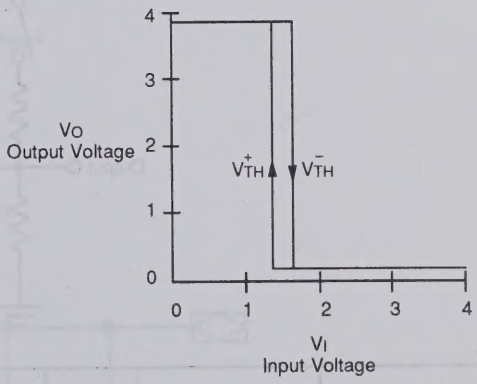


15559-015A

Input to Output Disable/Enable Through Transparent Latch



15559B-013B



15559B-014B

Notes:

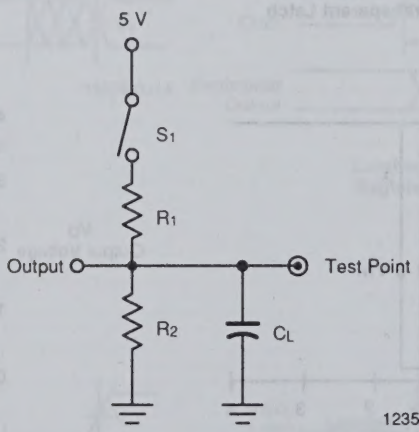
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12350-019A

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{PDL}, t_{CO}	Closed	50 pF	80 Ω	160 Ω	1.5 V
t_{PZX}, t_{EA}, t_{EAL}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}, t_{ERL}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

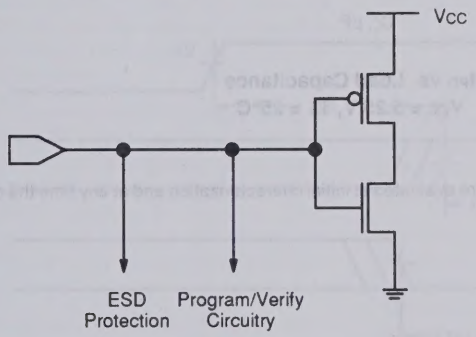
ENDURANCE CHARACTERISTICS

The PALCE16V8HD is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

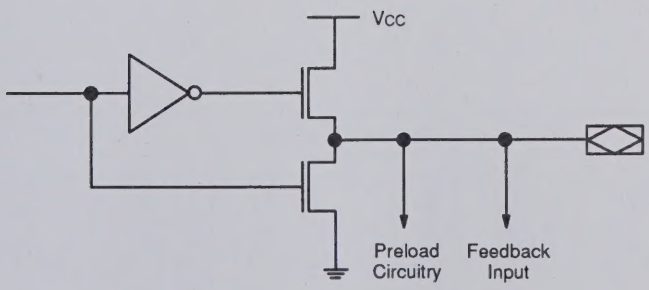
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



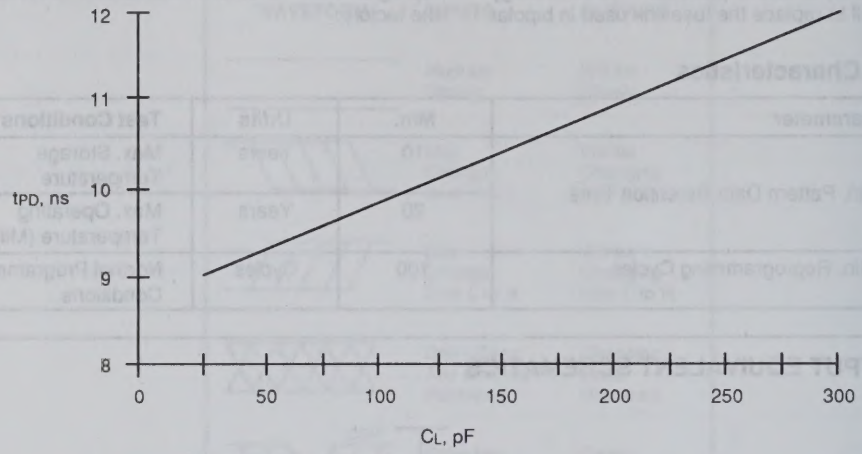
Typical Input



Typical Output

12197-013A

MEASURED SWITCHING CHARACTERISTICS for the PALCE16V8HD-15 (Note 1)



tPD vs. Load Capacitance
VCC = 5.25 V, TA = 25°C

14275-011A

Note:

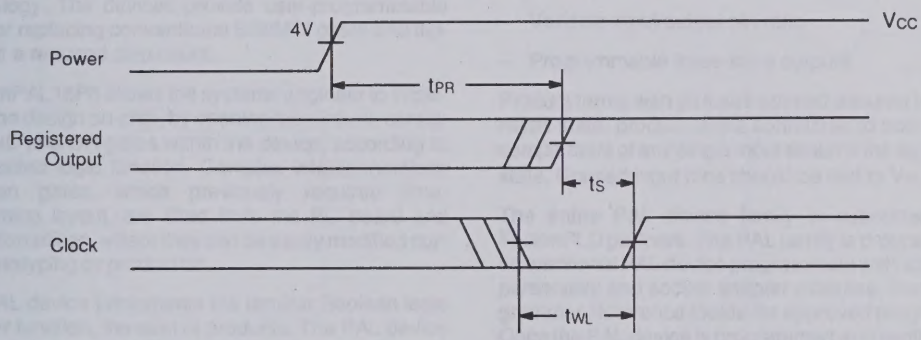
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where tPD may be affected.

POWER-UP RESET

The PALCE16V8HD has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

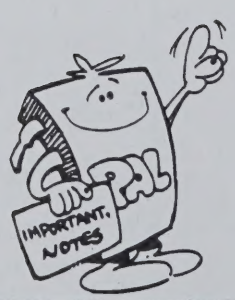
1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



12350-024A

Power-Up Reset Waveform


IMPORTANT
NOTES

AmPAL18P8B/AL/A/L

20-Pin Combinatorial TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 15 ns maximum propagation delay
- Universal combinatorial architecture
- Programmable output polarity
- Programmable replacement for high-speed TTL logic
- Extensive third–party software and programmer support through FusionPLD partners
- 20-pin DIP and 20-pin PLCC packages save space

GENERAL DESCRIPTION

The AmPAL18P8 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The AmPAL18P8 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

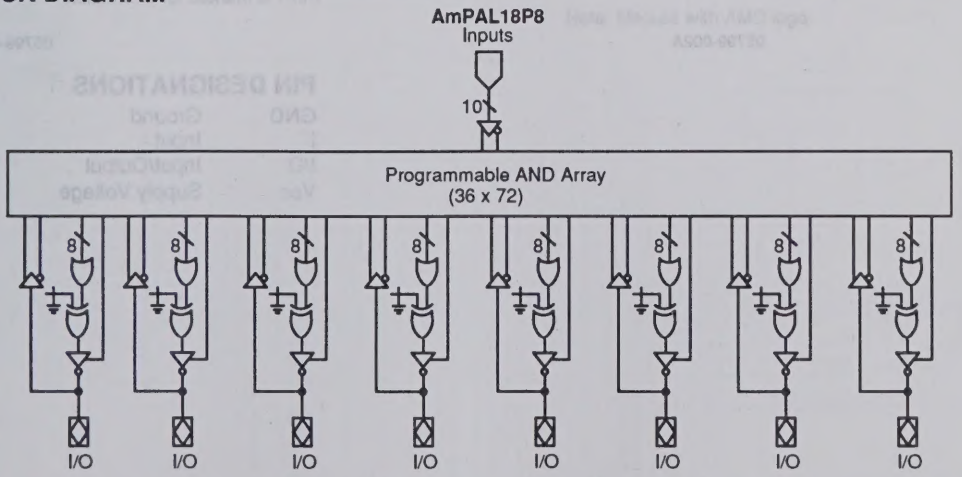
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

BLOCK DIAGRAM



05799-001A

Publication # 05799 Rev. G Amendment/0
Issue Date: January 1992

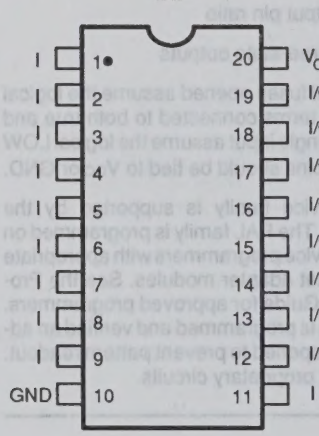
PRODUCT SELECTOR GUIDE

Family	t_{PD} ns (Max.)	I_{CC} mA (Max.)	I_{OL} mA (Min.)
Very High-Speed ("B") Versions	15	180	24
High-Speed ("A") Versions	25	180	24
High-Speed, Half-Power ("AL") Versions	25	90	24
Half-Power ("L") Versions	35	90	24

CONNECTION DIAGRAMS

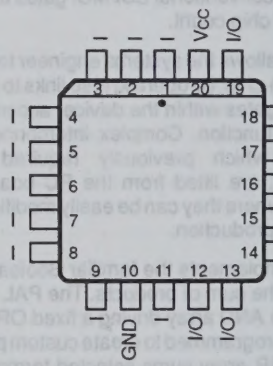
Top View

DIP



05799-002A

PLCC



Note:
Pin 1 is marked for orientation.

05799-003A

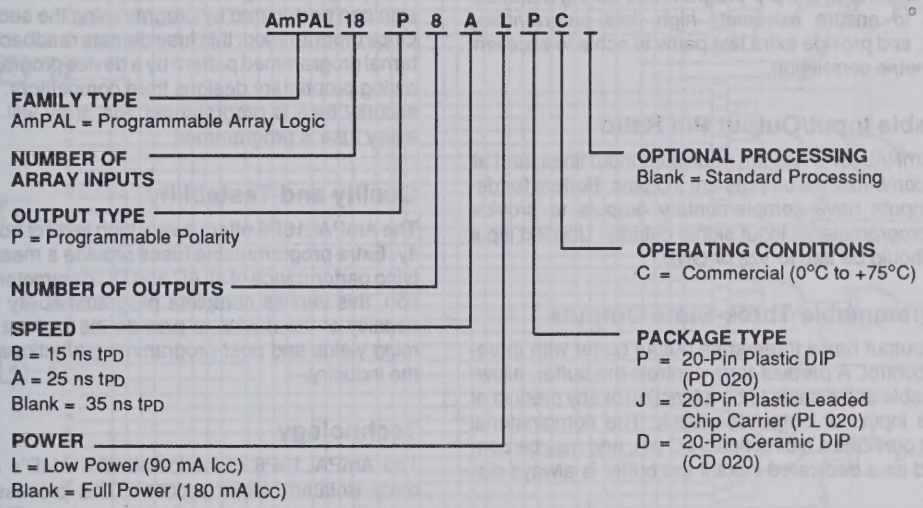
PIN DESIGNATIONS

GND	Ground
I	Input
I/O	Input/Output
V_{CC}	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
AmPAL18P8	B, AL, A, L	PC, JC, DC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The AmPAL18P8 has ten dedicated input lines, and all eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Polarity

The polarity of each output can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts. Selection is through a programmable fuse which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if the fuse is 1 (programmed) and active low if the fuse is 0 (intact).

Security Fuse

After programming and verification, an AmPAL18P8 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

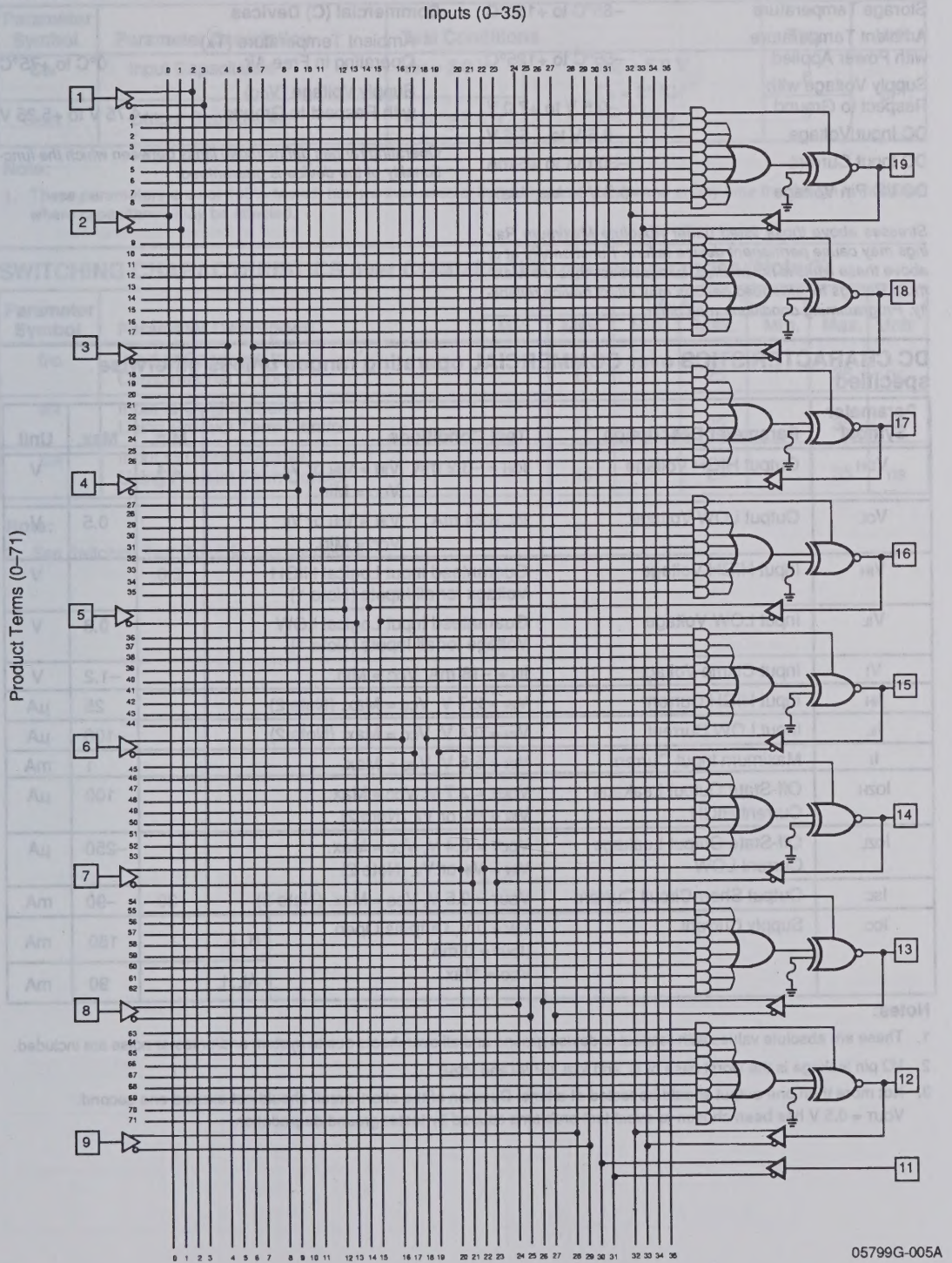
Quality and Testability

The AmPAL18P8 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The AmPAL18P8 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation.

LOGIC DIAGRAM



05799G-005A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to + 5.5 V
DC Input Current	–30 mA to +5 mA
DC I/O Pin Voltage	–0.5 V to V_{CC} Max.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–250	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	B, A		180	mA
			AL, L		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

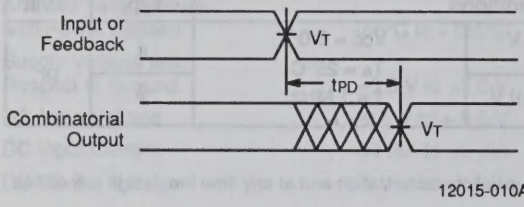
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	B		A, AL		L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output		15		25		35	ns
t_{EA}	Input to Output Enable Using Product Term Control		15		25		35	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		25		35	ns

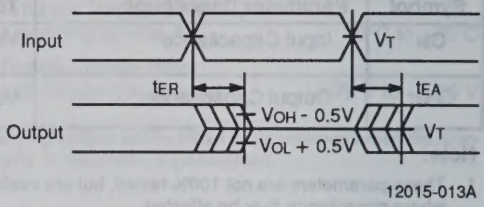
Note:

2. See Switching Test Circuit for test conditions.

SWITCHING WAVEFORMS



Combinatorial Output



Input to Output Disable/Enable

Notes:

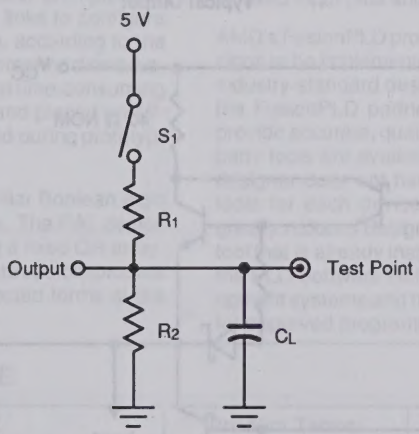
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

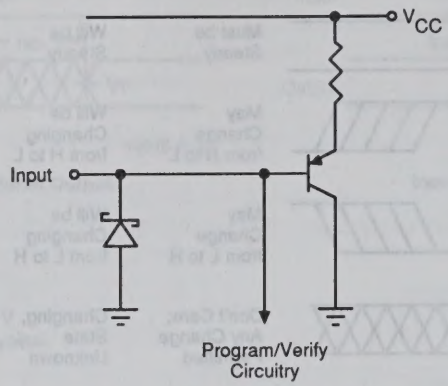


12350-019A

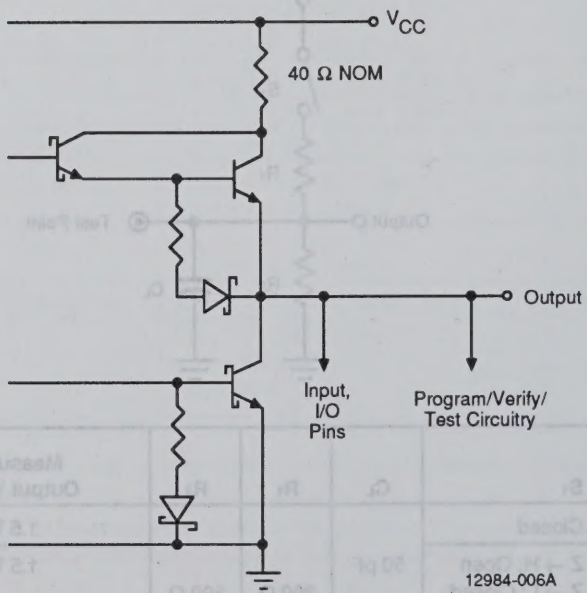
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output



PAL20R8 Family

24-Pin TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As fast as 5 ns maximum propagation delay**
- **Popular 24-pin architectures: 20L8, 20R8, 20R6, 20R4**
- **Programmable replacement for high-speed TTL logic**
- **Power-up reset for initialization**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The PAL20R8 Family (PAL20L8, PAL20R8, PAL20R6, PAL20R4) includes the PAL20R8-5 Series which is ideal for high-performance applications. The PAL20R8 Family is provided in the standard 24-pin DIP and 28-pin PLCC pinouts.

The family utilizes Advanced Micro Devices' advanced trench-isolated bipolar process and fuse-link technology. The devices provide user programmable logic for replacing conventional SSI/LSI gates and flip-flops at a reduced chip cost.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

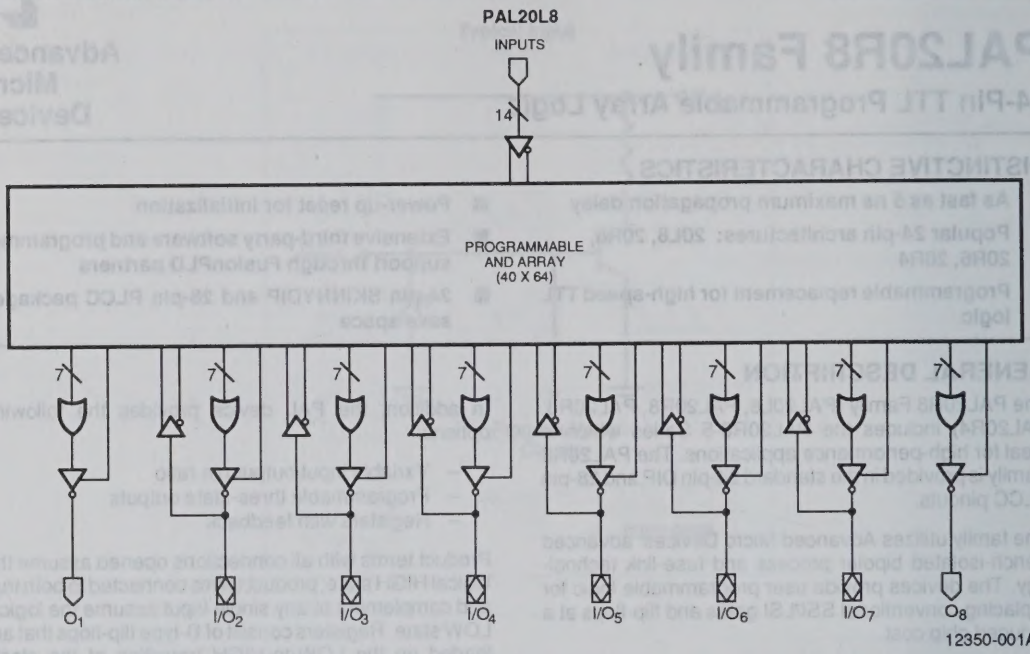
AMD's FusionPLD program allows PAL20R8 Family designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

PRODUCT SELECTOR GUIDE

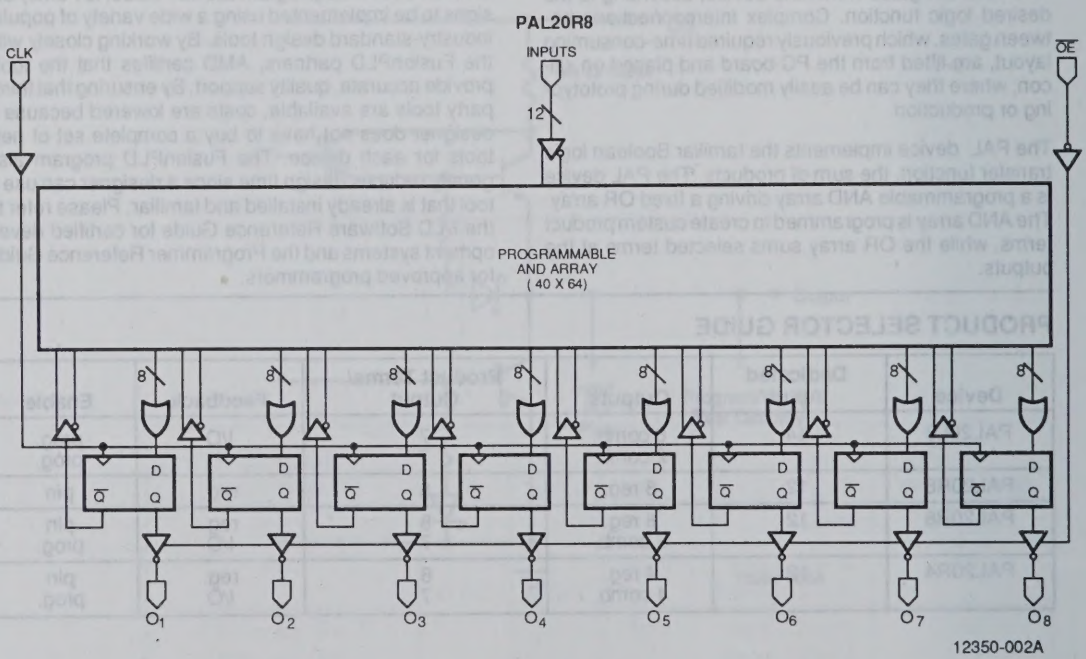
Device	Dedicated Inputs	Outputs	Product Terms/ Output	Feedback	Enable
PAL20L8	14	6 comb. 2 comb.	7 7	I/O –	prog. prog.
PAL20R8	12	8 reg.	8	reg.	pin
PAL20R6	12	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL20R4	12	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

Publication# 16490 Rev. A Amendment/0
Issue Date: January 1992

BLOCK DIAGRAMS

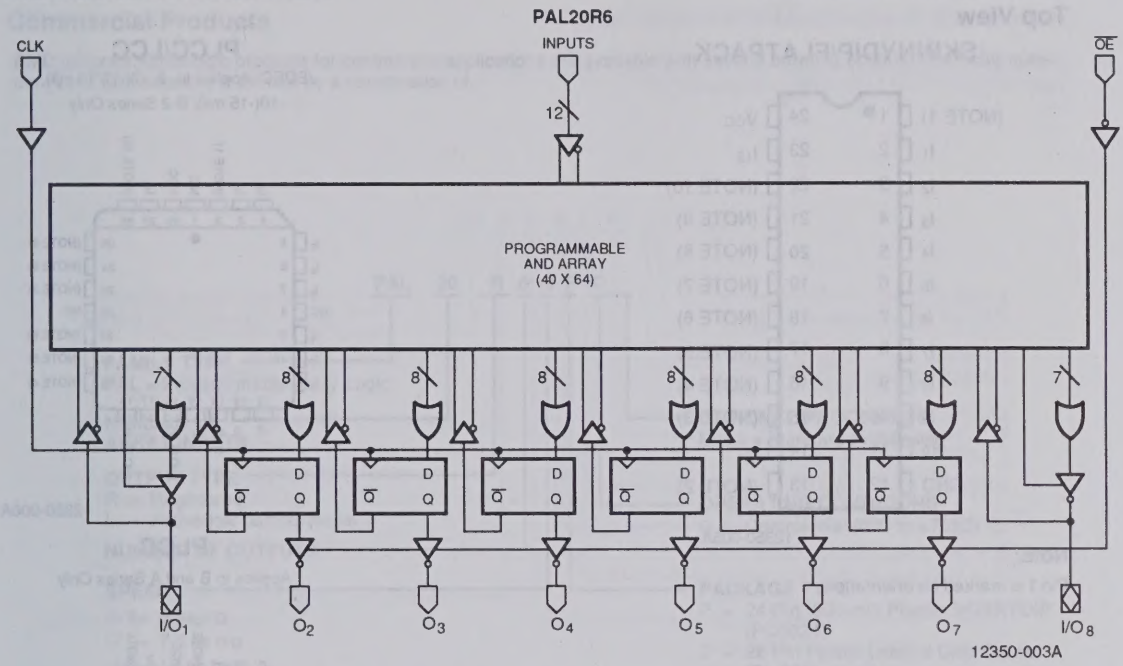


12350-001A



12350-002A

BLOCK DIAGRAMS



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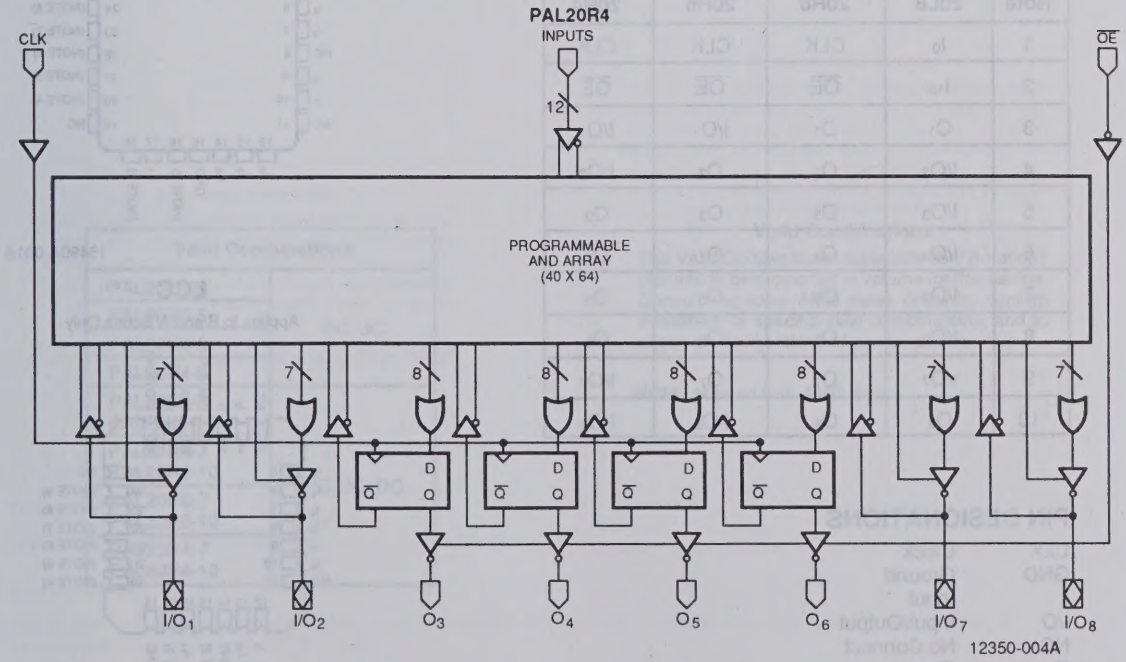
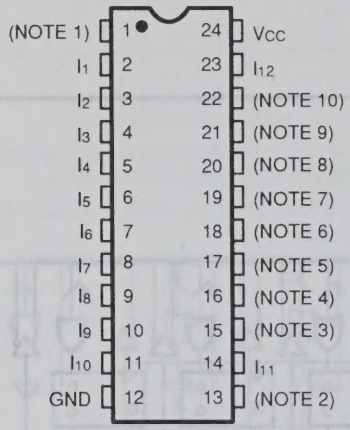


12350-004A

CONNECTION DIAGRAMS

Top View

SKINNYDIP/FLATPACK

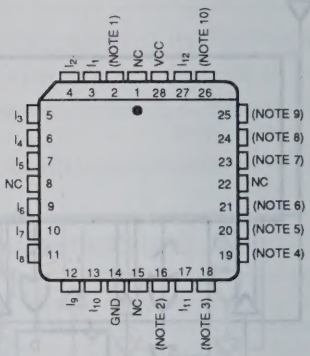


12350-005A

Note:
Pin 1 is marked for orientation.

PLCC/LCC

JEDEC: Applies to -5, -7(-12/10 mil), -10(-15 mil), B-2 Series Only



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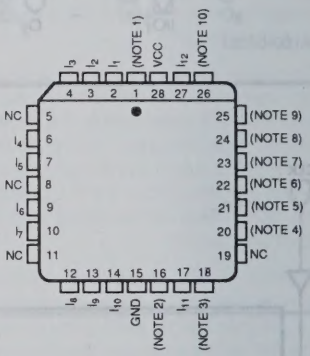
PLCC

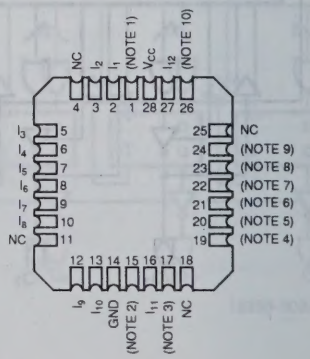
Applies to B and A Series Only



16490A-001A

LCC

Applies to B and A Series Only



16490A-002A

Note	20L8	20R8	20R6	20R4
1	I_0	CLK	CLK	CLK
2	I_{13}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
3	O_1	O_1	I/O_1	I/O_1
4	I/O_2	O_2	O_2	I/O_2
5	I/O_3	O_3	O_3	O_3
6	I/O_4	O_4	O_4	O_4
7	I/O_5	O_5	O_5	O_5
8	I/O_6	O_6	O_6	O_6
9	I/O_7	O_7	O_7	I/O_7
10	O_8	O_8	I/O_8	I/O_8

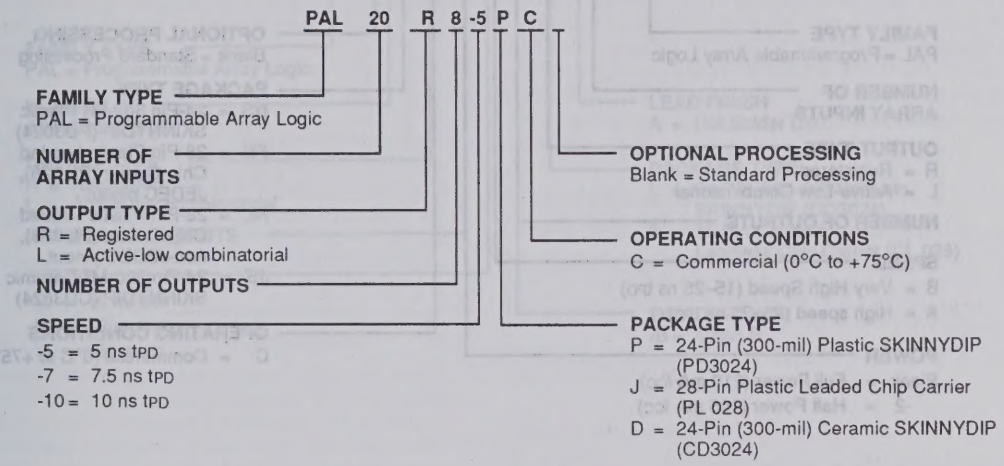
PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
O	Output
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL20L8-5	PC, JC
PAL20R8-5	
PAL20R6-5	
PAL20R4-5	
PAL20L8-7 PAL20L8-10	PC, JC, DC
PAL20R8-7 PAL20R8-10	
PAL20R6-7 PAL20R6-10	
PAL20R4-7 PAL20R4-10	

Valid Combinations

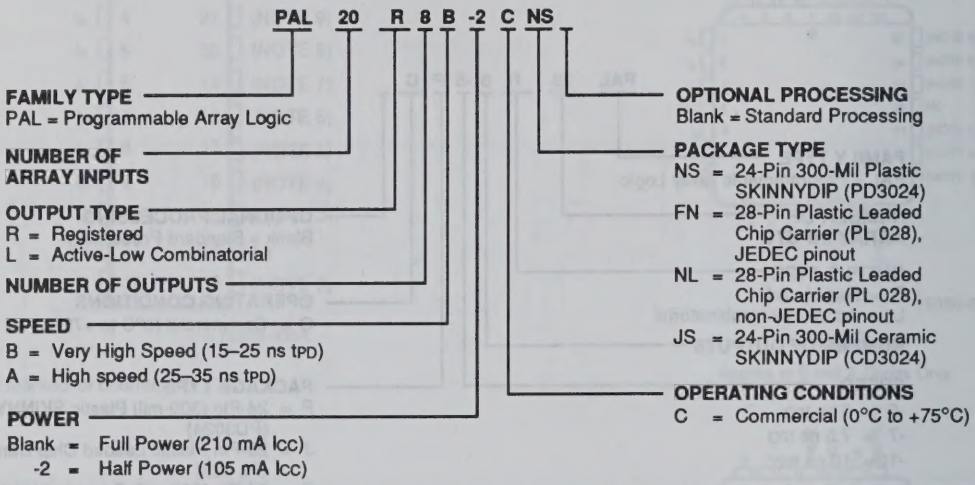
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION

Commercial Products (MMI Marking Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL20L8	B-2	CNS, CFN, CJS
PAL20R8 PAL20R6 PAL20R4	B, A	CNS, CNL, CJS

Valid Combinations

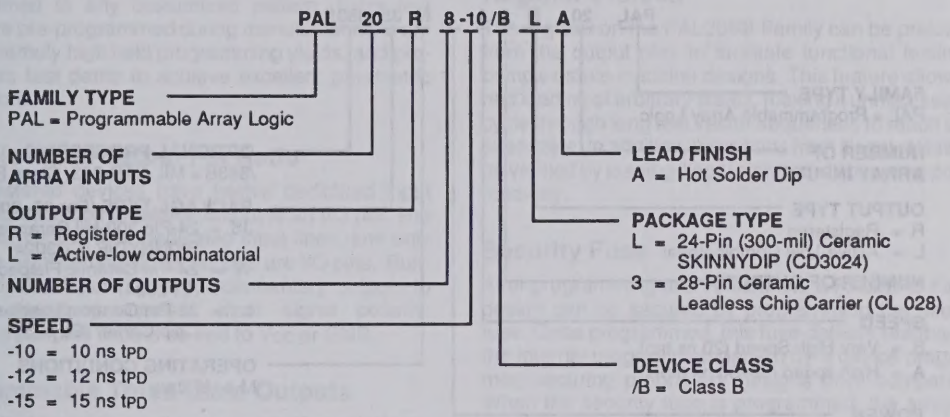
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL20L8 PAL20R8 PAL20R6 PAL20R4	-10, -12, -15	/BLA, /B3A

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

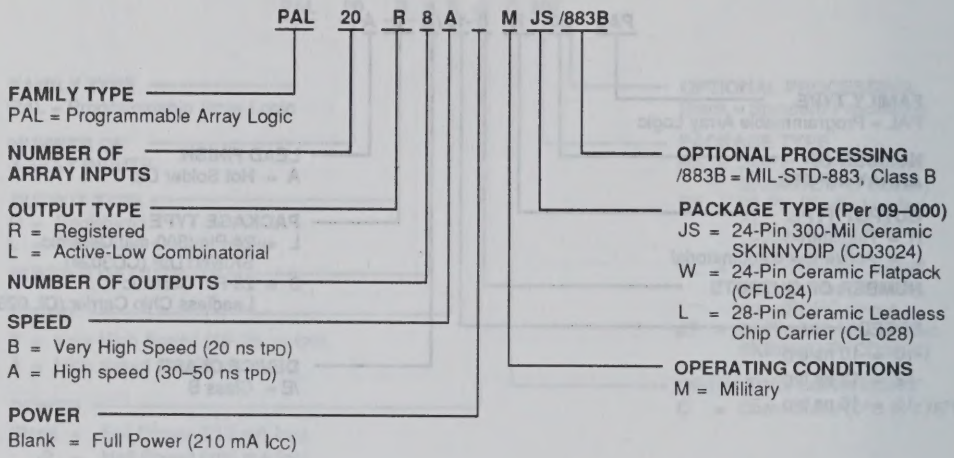
Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

ORDERING INFORMATION
APL Products (MMI Marking Only)

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PAL20L8	B, A	MJS/883B, MW/883B, ML/883B
PAL20R8		
PAL20R6		
PAL20R4		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

Standard 24-Pin PAL Family

The standard 24-pin PAL family is comprised of four different devices, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Using any of a number of development packages, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have twelve dedicated input lines, and each combinatorial output is an I/O pin. The PAL20L8 has fourteen dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20R8 Family will be HIGH due to the active-low outputs. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL20R8 Family can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL20R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is intact.

Quality and Testability

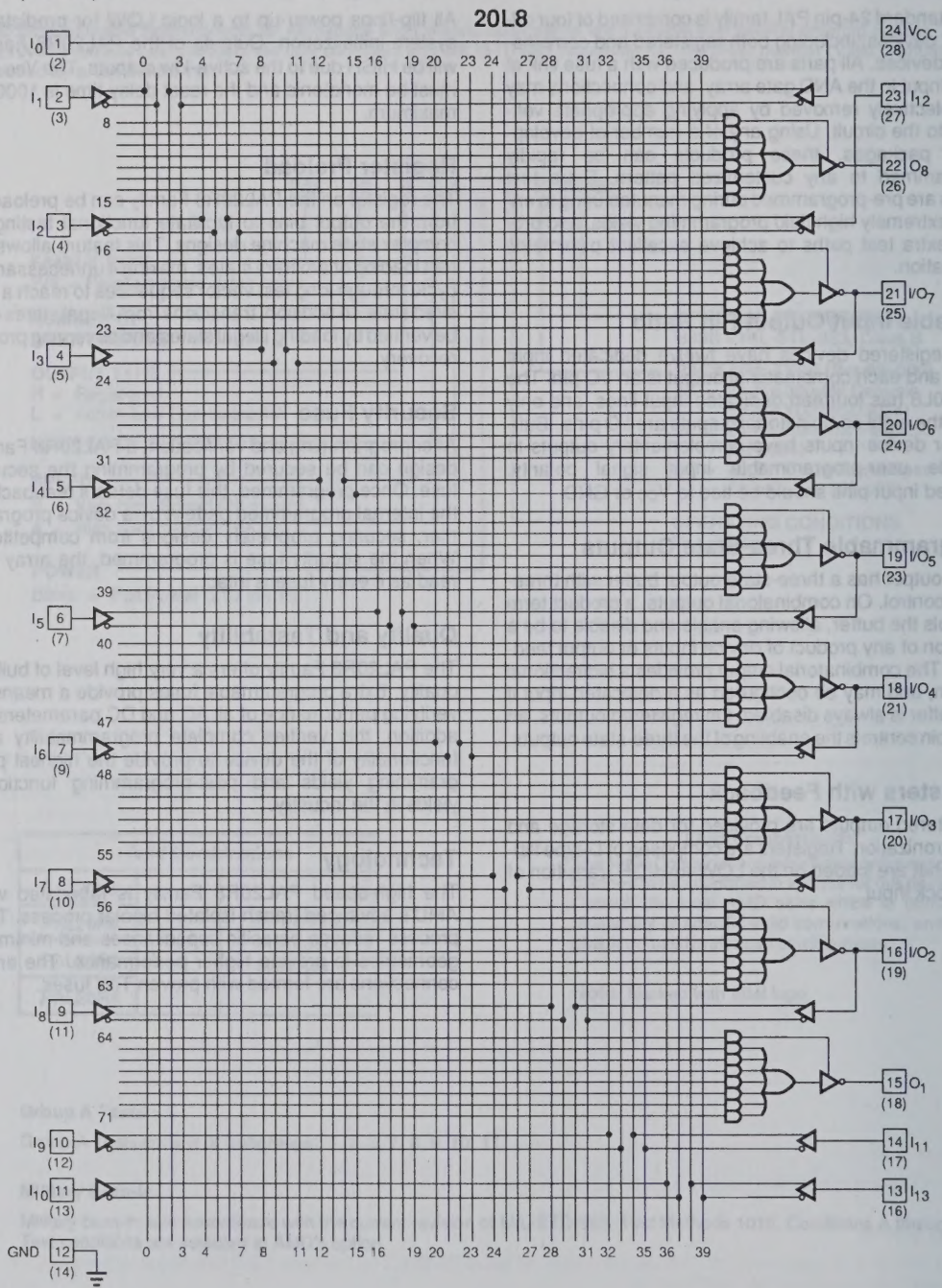
The PAL20R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PAL20R8 Family is fabricated with AMD's advanced trench-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses.

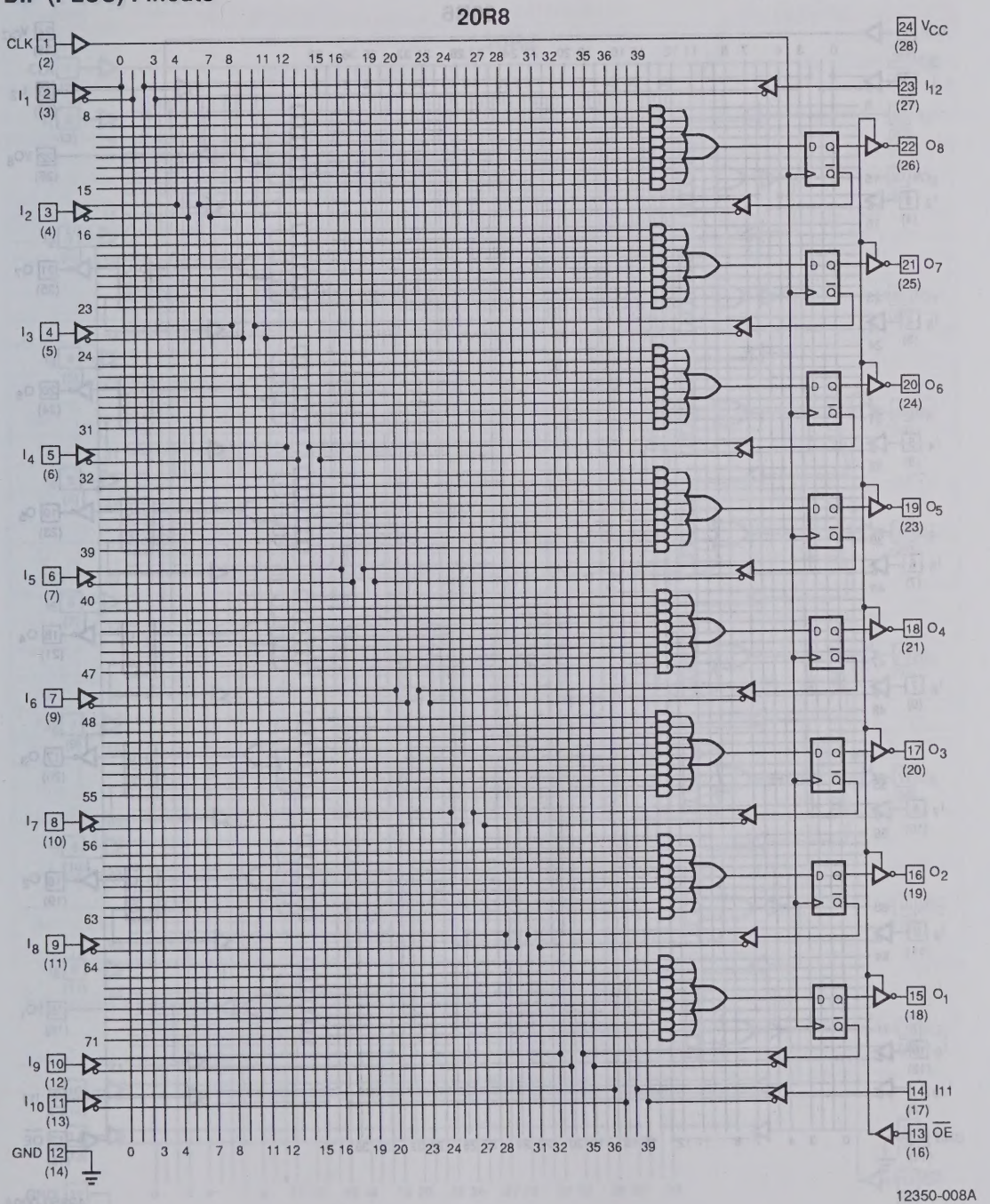
LOGIC DIAGRAM

DIP (PLCC) Pinouts



12350-007A

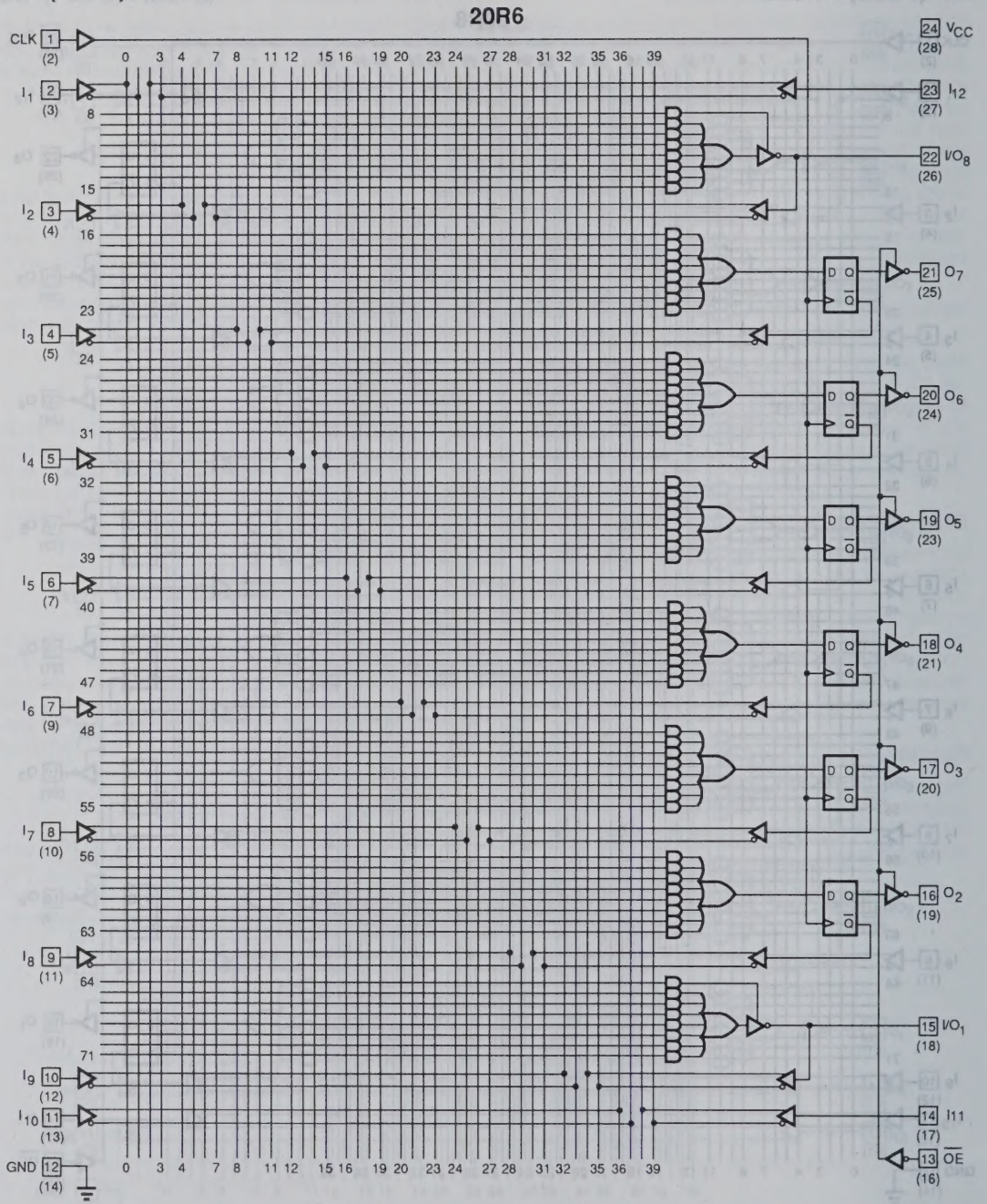
LOGIC DIAGRAM
DIP (PLCC) Pinouts



12350-008A

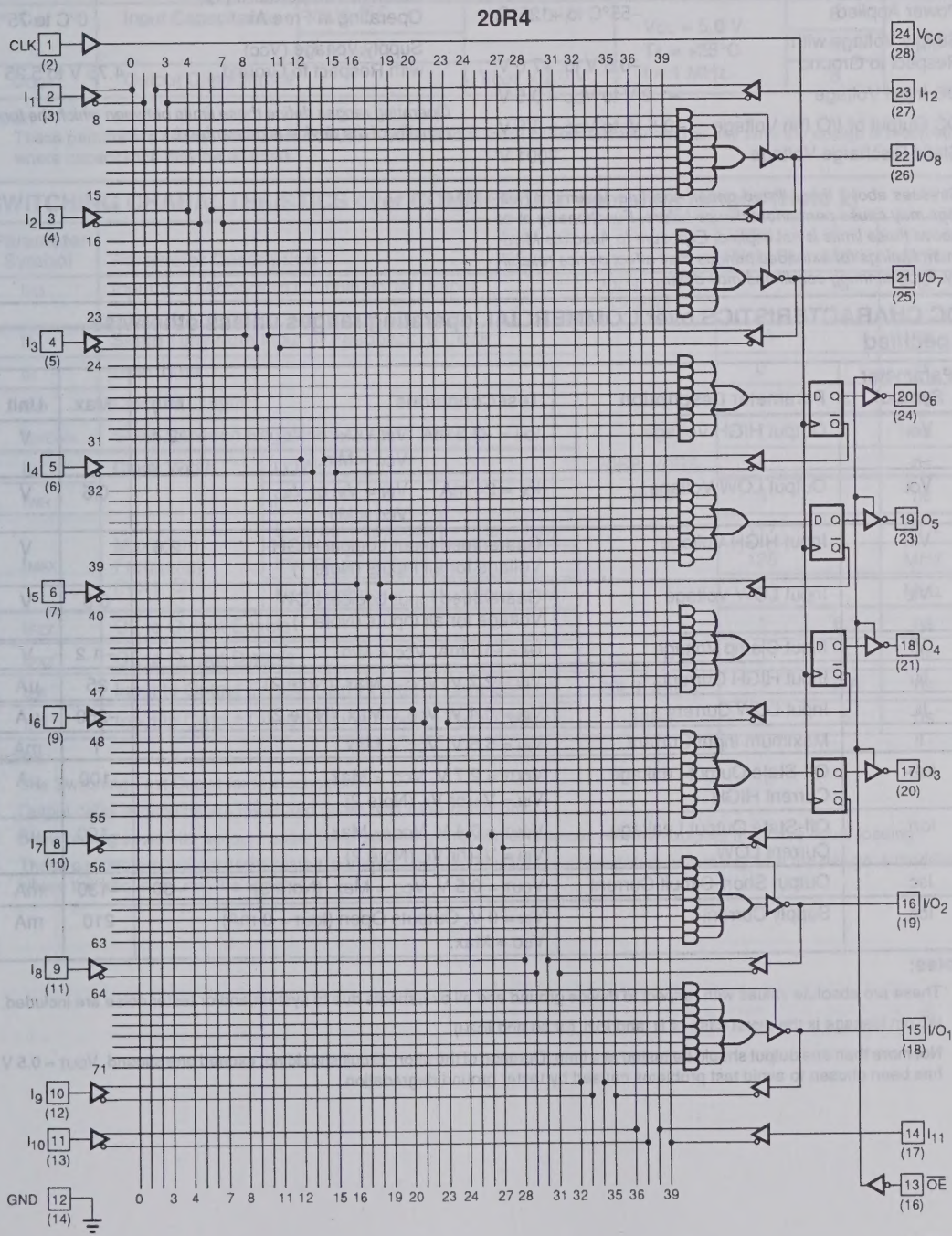
LOGIC DIAGRAM

DIP (PLCC) Pinouts



12350-009A

LOGIC DIAGRAM
DIP (PLCC) Pinouts



12350-010A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to 75°C
Supply Voltage (V_{CC}) with Respect to Ground	4.75 V to 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	CLK, $\overline{OE}$	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	8	pF
		$I_1 - I_{12}$			5	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	1	5	ns
t_S	Setup Time from Input or Feedback to Clock				4.5		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				1	4	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 4)					1	ns
t_{WL}	Clock Width	LOW		20R8, 20R6, 20R4	4		ns
t_{WH}		HIGH			4		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		117		MHz
		Internal Feedback (f_{CNT})			125		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		125		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	6.5	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	5	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4	2	6.5	ns
t_{ER}	Input to Output Disable Using Product Term Control				2	5	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) With Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		−250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	3	7.5	ns
		1 Output Switching			3	7	
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	7		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				3	6.5	ns
t_{SKEW}	Skew Between Registered Outputs (Note 4)					1	ns
t_{WL}	Clock Width	LOW			5		ns
t_{WH}		HIGH			5		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		74		MHz
		Internal Feedback (f_{CNT})			100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		100		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				3	8	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				3	8	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control				3	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Skew is measured with all outputs switching in the same direction.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V	CLK, $\overline{OE}$	12	pF
			T_A = 25°C	Other Inputs	7	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	Outputs	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	3	10	ns
t_S	Setup Time from Input or Feedback to Clock				10		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output			20R8, 20R6,	2	8	ns
t_{WL}	Clock Width	LOW		20R4	7		ns
t_{WH}		HIGH			7		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		55.5		MHz
		Internal Feedback (f_{CNT})			58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		71.4		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				1	10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				1	10	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6,	3	10	ns
t_{ER}	Input to Output Disable Using Product Term Control			20R4	3	10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		15	ns
t_S	Setup Time from Input or Feedback to Clock				15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback			20R8, 20R6,		12	ns
t_{WL}	Clock Width	LOW		20R4	10		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		45		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					12	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6,		18	ns
t_{ER}	Input to Output Disable Using Product Term Control			20R4		15	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback (f_{CNT})			28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. Calculated from measured f_{MAX} internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		25	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	25		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					15	ns
t_{WL}	Clock Width	LOW			15		ns
t_{WH}		HIGH			15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$		25		MHz
		Internal Feedback (f_{CNT})			28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		33		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					20	ns
t_{EA}	Input to Output Enable Using Product Term Control			20L8, 20R6, 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control					25	ns

Notes:

1. See Switching Test Circuit for test conditions.
2. Calculated from measured f_{MAX} internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature With Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case (T_C) Temperature	–55°C to +125°C
Supply Voltage (V_{CC}) With Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are 100% tested at T_C = +25 °C , +125 °C, and –55°C.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		10	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				-10 Min. (Note 3)	-10 Max.	-12 Min. (Note 3)	-12 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	3	10	3	12	ns
t_S	Setup Time from Input or Feedback to Clock				10		12		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output				3	10	3	12	ns
t_{SKEW}	Skew Between Registered Outputs (Note 4)					1		1	ns
t_{WL}	Clock Width	LOW		20R8, 20R6, 20R4	8		10		ns
t_{WH}		HIGH			8		10		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		50		41.7		MHz
		Internal Feedback (f_{CNT})			62.5		50		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		62.5		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 5)				3	12	3	15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 5)				3	12	3	15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)			20L8, 20R6, 20R4	3	12	3	15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				3	12	3	15	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
4. Skew is measured with all outputs switching in the same direction.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions			Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V	CLK, $\overline{OE}$	12	pF
			T_A = 25°C	Other Inputs	7	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	Outputs	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4	3	15	ns
t_S	Setup Time from Input or Feedback to Clock				15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output				2	13	ns
t_{WL}	Clock Width	LOW		20R8, 20R6, 20R4	10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$		35.7		MHz
		Internal Feedback (f_{CNT})			37		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 6)				1	15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 6)				1	15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 6)			20L8, 20R6, 20R4	3	15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 6)				3	15	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Minimum value for t_{PD}, t_{CO}, t_{PZX}, t_{PXZ}, t_{EA}, and t_{ER} parameters should be used for simulation purposes only and are not tested.
4. Calculated from measured f_{MAX} internal.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to + 5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		20	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	20		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					15	ns
t_{WL}	Clock Width	LOW			12		ns
t_{WH}		HIGH			12		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		28.5		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6, 20R4		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					20	ns

Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	+125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

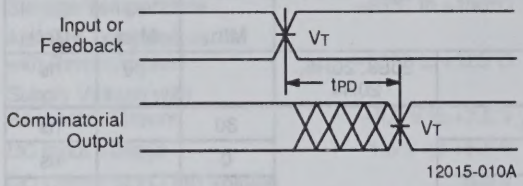
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 1)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6, 20R4		30	ns
t_S	Setup Time from Input or Feedback to Clock			20R8, 20R6, 20R4	30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					20	ns
t_{WL}	Clock Width	LOW			20		ns
t_{WH}		HIGH			20		ns
f_{MAX}	Maximum Frequency (Note 2)	External Feedback	$1/(t_S + t_{CO})$		20		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$		25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)					25	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)					25	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6, 20R4		30	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)					30	ns

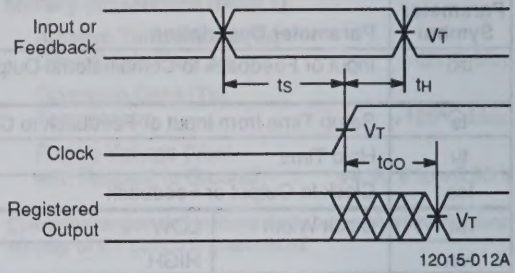
Notes:

1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

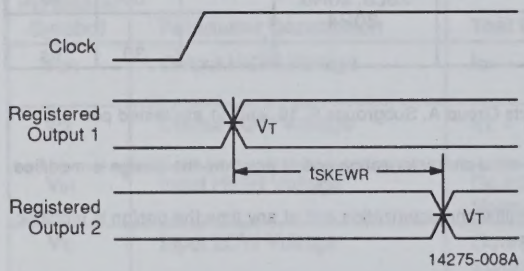
SWITCHING WAVEFORMS



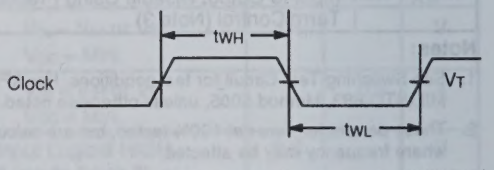
Combinatorial Output



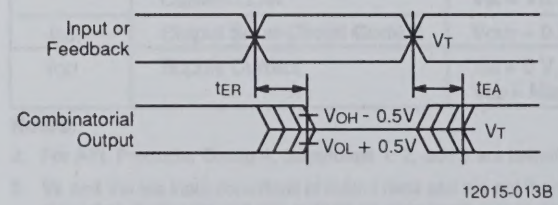
Registered Output



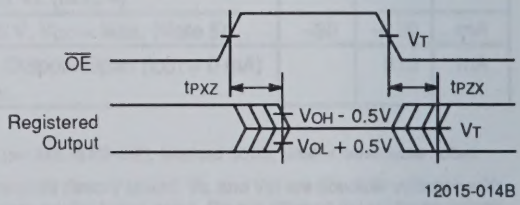
Registered Output Skew



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

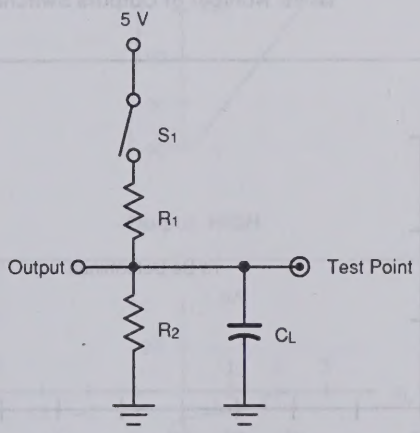
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–3 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

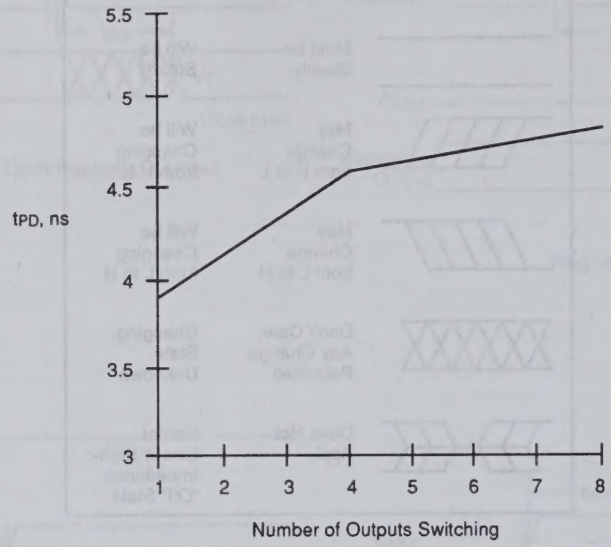


12350-019A

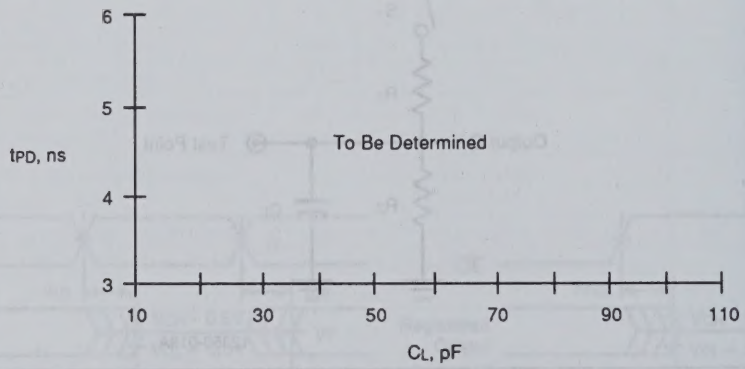
Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	200 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

MEASURED SWITCHING CHARACTERISTICS FOR THE PAL20R8-5

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching 10294-005B



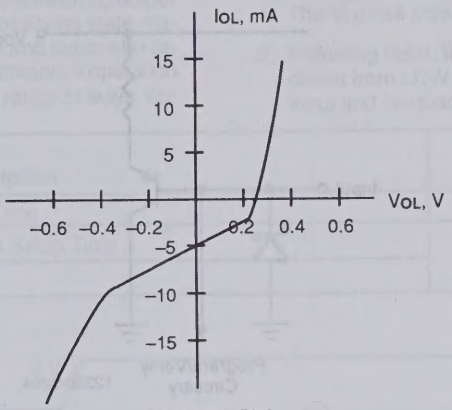
t_{PD} vs. Load Capacitance 10294-006A

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.

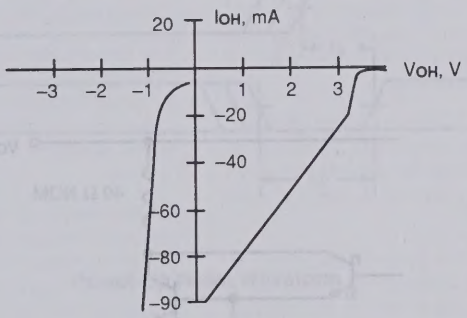
CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS FOR THE PAL20R8-5

V_{CC} = 5.0 V, T_A = 25°C



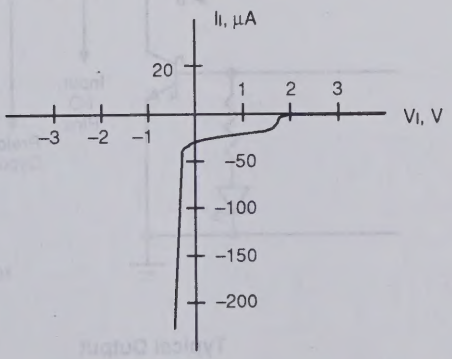
Output, LOW

10240-003B



Output, HIGH

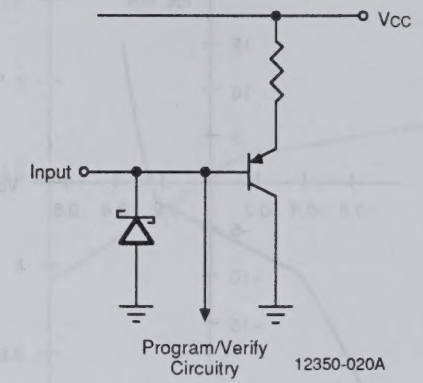
10240-004B



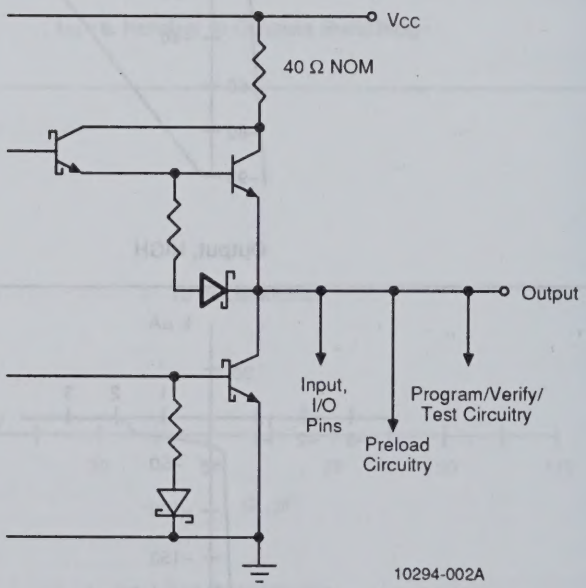
Input

10240-005A

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



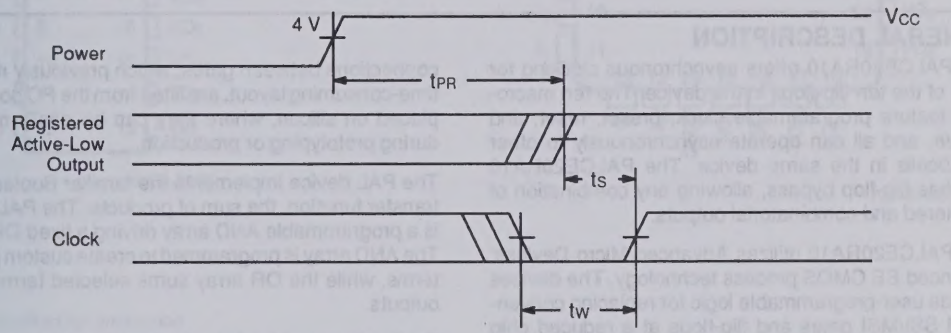
Typical Output

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

PALCE20RA10H-15

24-Pin Asynchronous EE CMOS Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Low power at 90 mA I_{CC}
- 15 ns maximum propagation delay and 50 MHz f_{MAX}
- Individually programmable asynchronous clock, preset, reset, and enable
- Registered or combinatorial outputs
- Programmable polarity
- Programmable replacement for high-speed CMOS or TTL logic
- TTL-level register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The PALCE20RA10 offers asynchronous clocking for each of the ten flip-flops in the device. The ten macrocells feature programmable clock, preset, reset, and enable, and all can operate asynchronously to other macrocells in the same device. The PALCE20RA10 also has flip-flop bypass, allowing any combination of registered and combinatorial outputs.

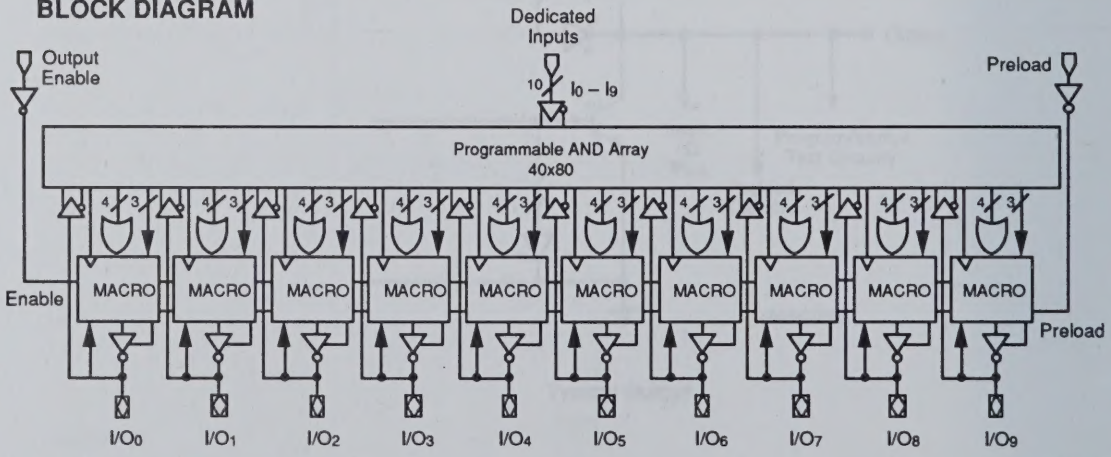
The PALCE20RA10 utilizes Advanced Micro Devices' advanced EE CMOS process technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PALCE20RA10 allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

Product terms with all inputs disconnected assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V_{CC} or GND.

BLOCK DIAGRAM

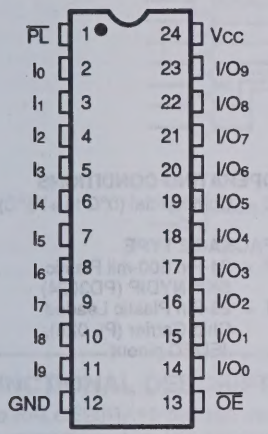


10243-001A

Publication# 15434 Rev. B Amendment/0
Issue Date: January 1992

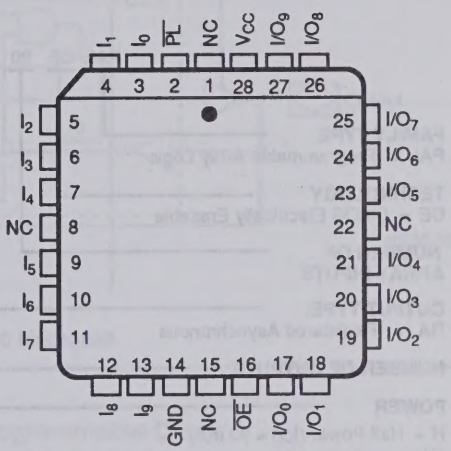
CONNECTION DIAGRAMS
Top View

SKINNYDIP/FLATPACK



12350-002A

PLCC



10243-003A

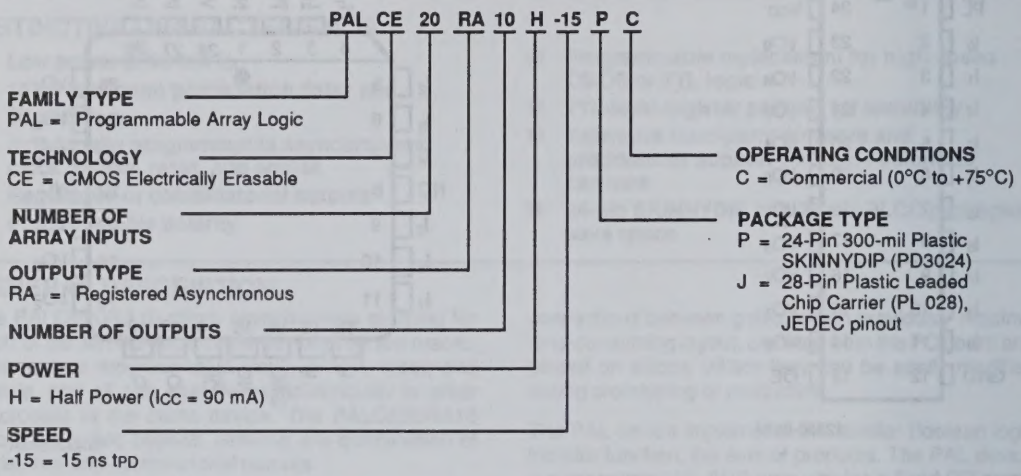
Note:
Pin 1 is marked for orientation

PIN DESIGNATIONS

GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
$\overline{OE}$	Output Enable
$\overline{PL}$	Preload
Vcc	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE20RA10H-15	PC, JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

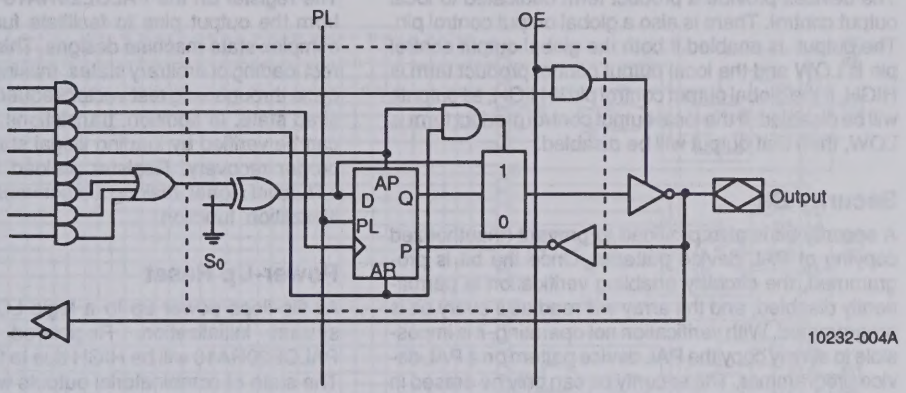


Figure 1. PALCE20RA10 Macrocell

FUNCTIONAL DESCRIPTION

The PALCE20RA10 has ten dedicated input lines and ten programmable I/O macrocells. The Registered Asynchronous (RA) macrocell is shown in Figure 1. Pin 1 serves as global register preload and pin 13 serves as global output enable. Programmable output polarity is available to provide user-programmable output polarity for each individual macrocell.

The programmable functions in the PALCE20RA10 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

Programmable Preset and Reset

In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product line is HIGH, the Q output of the register becomes a logic 1. If the reset product line is HIGH, the Q output of the register becomes a logic 0. The operation of the programmable preset and reset overrides the clock.

Combinatorial/Registered Outputs

If both the preset and reset product lines are HIGH, the flip-flop is bypassed and the output becomes combinatorial. Otherwise, the output is from the register. Each output can be configured to be combinatorial or registered.

Programmable Clock

The clock input to each flip-flop comes from the programmable array, allowing any flip-flop to be clocked independently if desired.

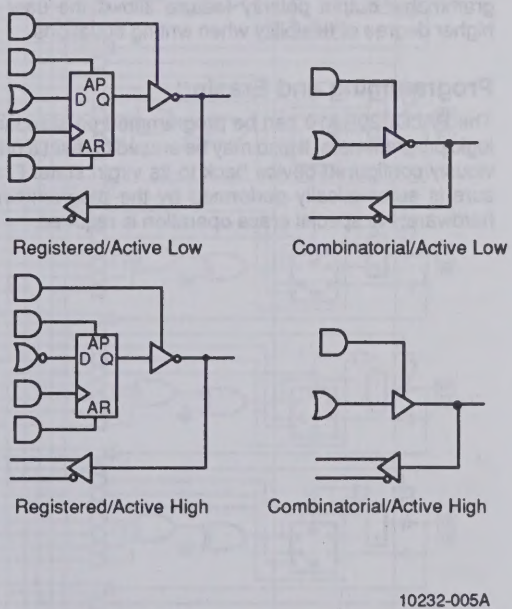


Figure 2. Macrocell Configurations

Three-State Outputs

The devices provide a product term dedicated to local output control. There is also a global output control pin. The output is enabled if both the global output control pin is LOW and the local output control product term is HIGH. If the global output control pin is HIGH, all outputs will be disabled. If the local output control product term is LOW, then that output will be disabled.

Security Bit

A security bit is also provided to prevent unauthorized copying of PAL device patterns. Once the bit is programmed, the circuitry enabling verification is permanently disabled, and the array will read as if every bit is programmed. With verification not operating, it is impossible to simply copy the PAL device pattern on a PAL device programmer. The security bit can only be erased in conjunction with the entire pattern.

Programmable Polarity

The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the PALCE20RA10 logic diagram. When the output polarity bit is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity bit is unprogrammed, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

Programming and Erasing

The PALCE20RA10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Register Preload

The register on the PALCE20RA10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transistions from illegal states can be verified by loading illegal states and observing proper recovery. Register preload is controlled by a TTL-level signal, making it a convenient board-level initialization function.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Registered outputs of the PALCE20RA10 will be HIGH due to the output inverter. The state of combinatorial outputs will be a function of the logic.

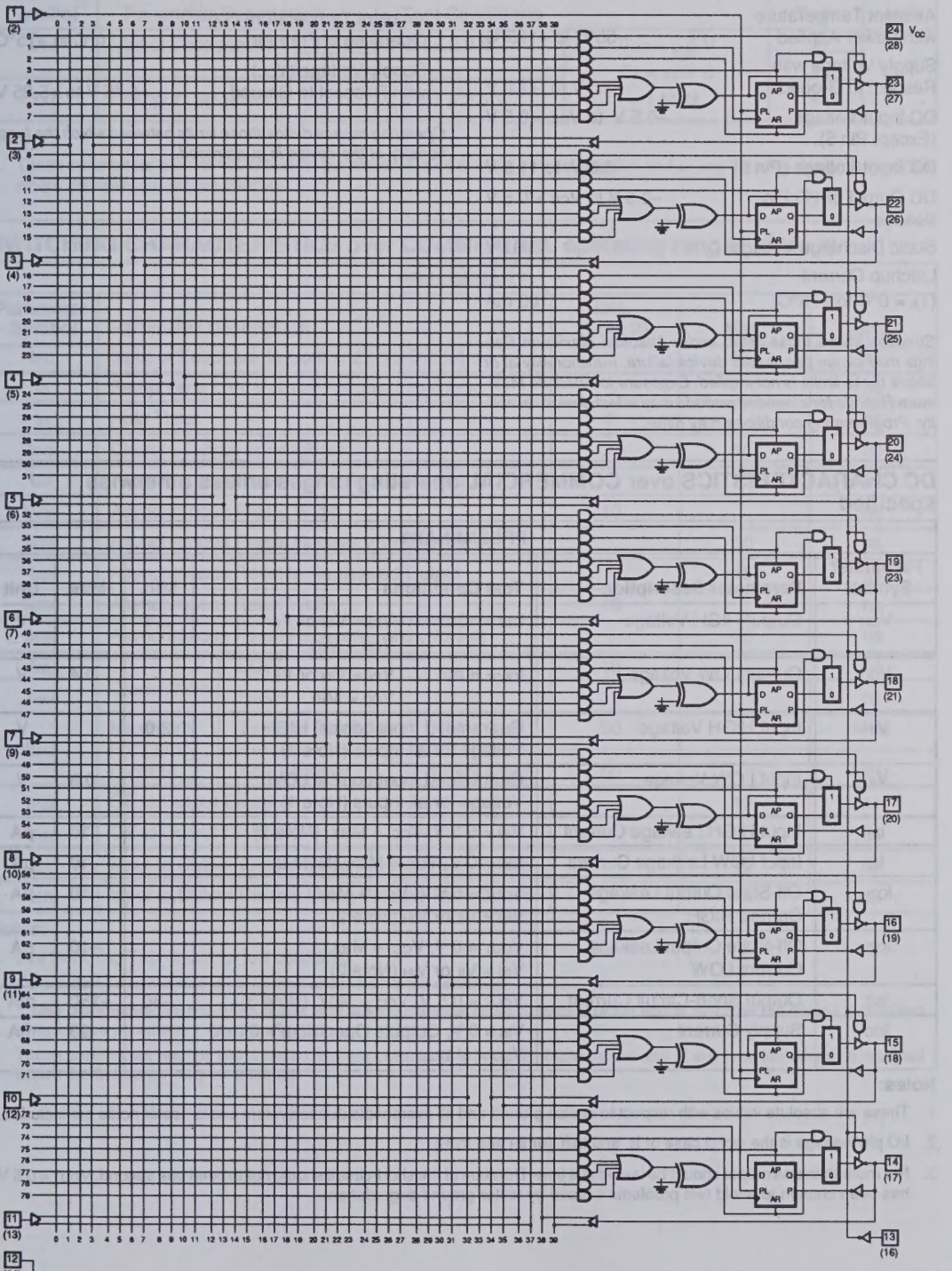
Quality and Testability

The PALCE20RA10 offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE20RA10H-15 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
DIP (PLCC) Pinouts



10243-007B

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage (Except Pin 5)	−0.5 V to V_{CC} + 0.5 V
DC Input Voltage (Pin 5)	−0.6 V to 11.0 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)		−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−150	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1) (-20 only)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Inputs	V_{IN} = 2.0 V	V_{CC} = 5.0 V	5	pF
		$\overline{OE}$		T_A = +25°C	9	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

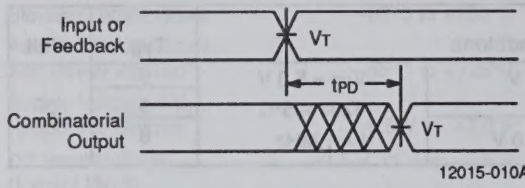
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

PRELIMINARY						
Parameter Symbol	Parameter Description			Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input or Feedback to Clock			5		ns
t_H	Hold Time			2		ns
t_{CO}	Clock to Output or Feedback				15	ns
t_{AP}	Asynchronous Preset to Registered Output				15	ns
t_{APW}	Asynchronous Preset Width			10		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)				10	ns
t_{AR}	Asynchronous Reset to Registered Output				15	ns
t_{ARW}	Asynchronous Reset Width			10		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				10	ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Note 5)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	50		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				10	ns
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

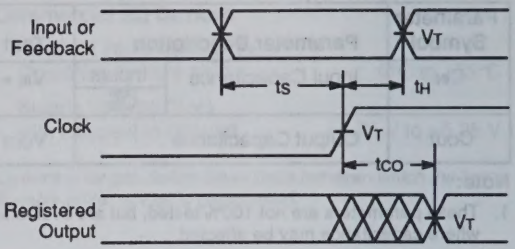
Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

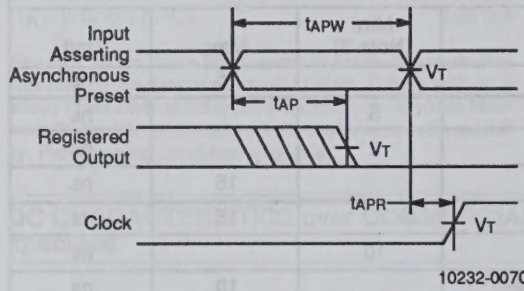
SWITCHING WAVEFORMS



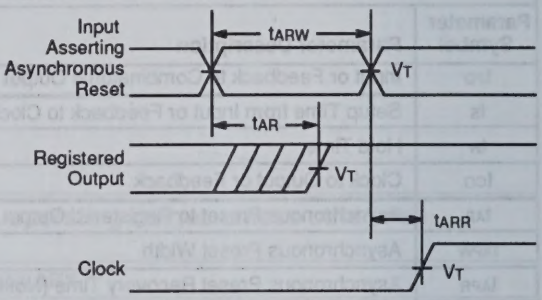
Combinatorial Output



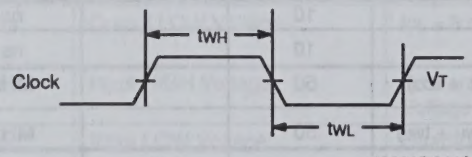
Registered Output



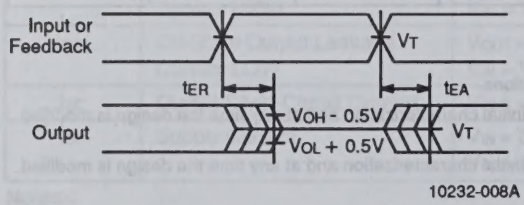
Asynchronous Preset



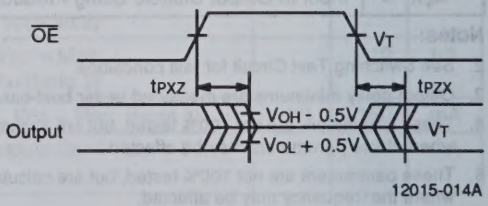
Asynchronous Reset



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

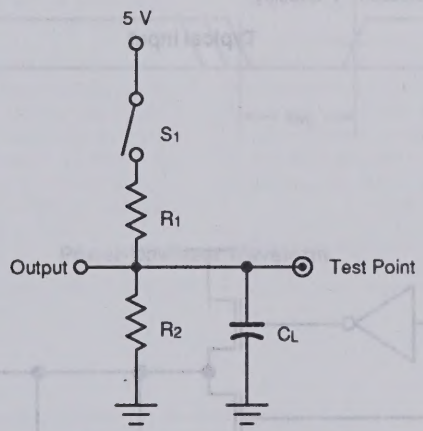
1. $V_T = 1.5$ V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12350-019A

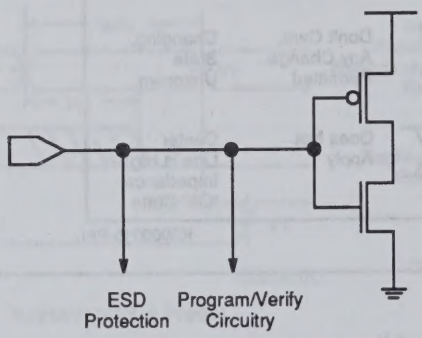
Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	560 Ω	1.1K Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

ENDURANCE CHARACTERISTICS

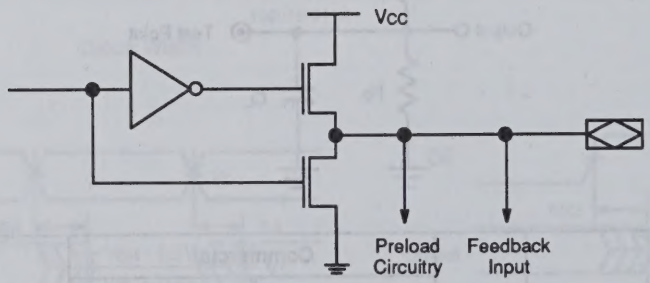
The PALCE20RA10 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

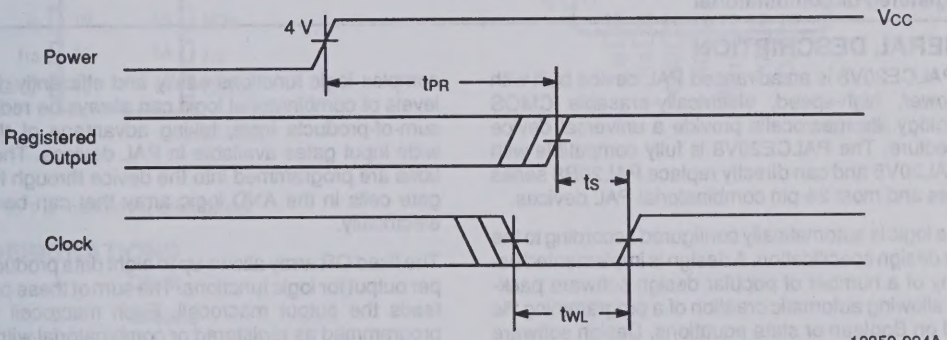
12197-013A

POWER-UP RESET

The PALCE20RA10 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol		Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

PALCE20V8 Family

EE CMOS 24-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Pin, function and fuse-map compatible with all GAL 20V8/As**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - -10 ns propagation delay for "-10" version
  - -15 ns propagation delay for "-15" version
- **Direct plug-in replacement for a wide range of 24-pin PAL devices**
- **Outputs individually programmable as registered or combinatorial**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
  Automatic register reset on power-up
- **Cost-effective 24-pin plastic SKINNYDIP and 28-pin PLCC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

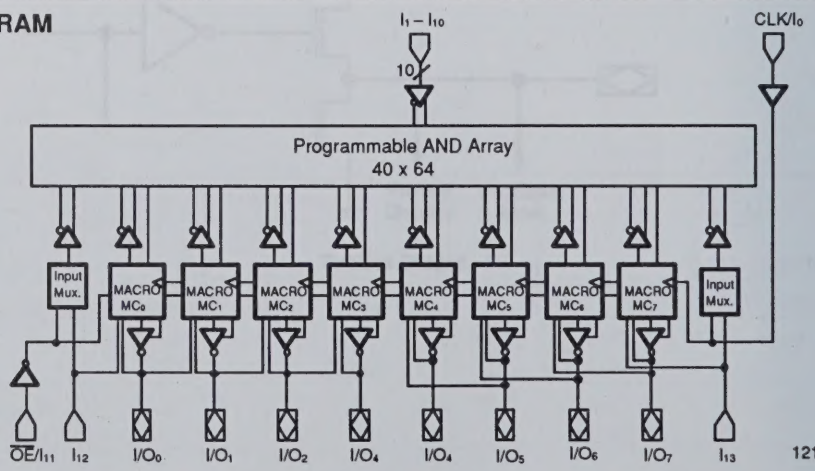
The PALCE20V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture. The PALCE20V8 is fully compatible with the GAL20V8 and can directly replace PAL20R8 series devices and most 24-pin combinatorial PAL devices.

Device logic is automatically configured according to the user's design specification. A design is implemented using any of a number of popular design software packages, allowing automatic creation of a programming file based on Boolean or state equations. Design software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE20V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

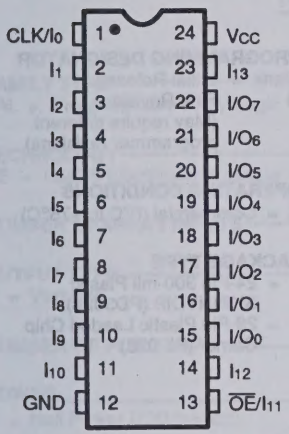
BLOCK DIAGRAM



Publication# 16491 Rev. A Amendment/0
Issue Date: January 1992

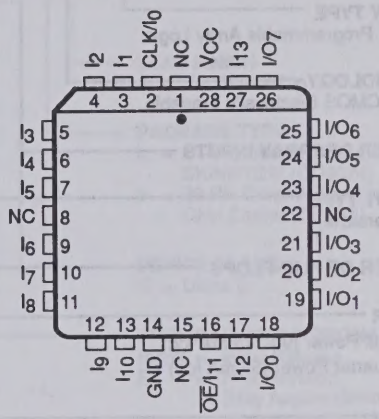
CONNECTION DIAGRAMS
(Top View)

SKINNYDIP



12197-002B

PLCC/LCC



12197-003A

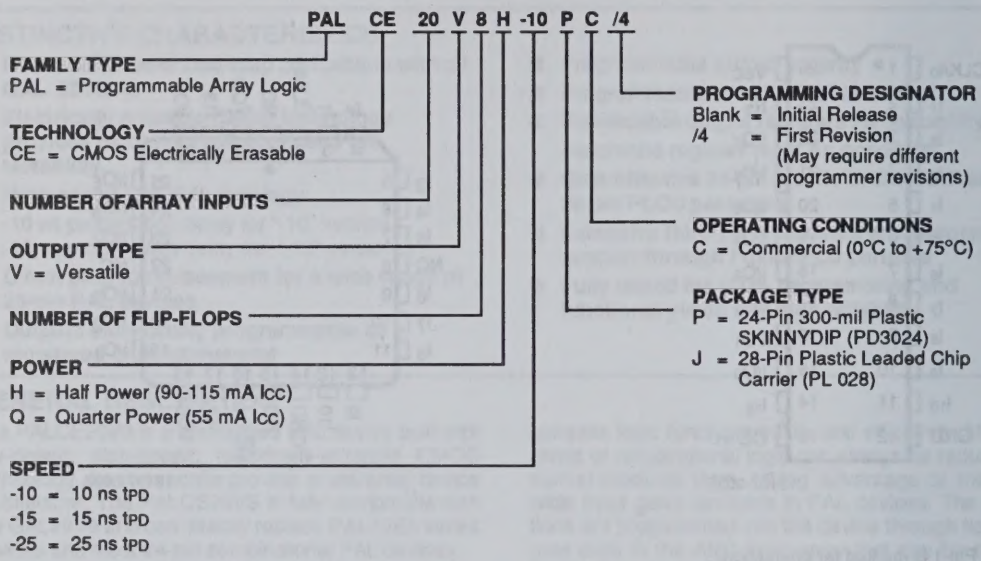
Note: Pin 1 is marked for orientation.

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
$\overline{OE}$	=	Output Enable
Vcc	=	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE20V8H-10	PC, JC	/4
PALCE20V8H-15		Blank, /4
PALCE20V8H-25		
PALCE20V8Q-15		
PALCE20V8Q-25		

Valid Combinations

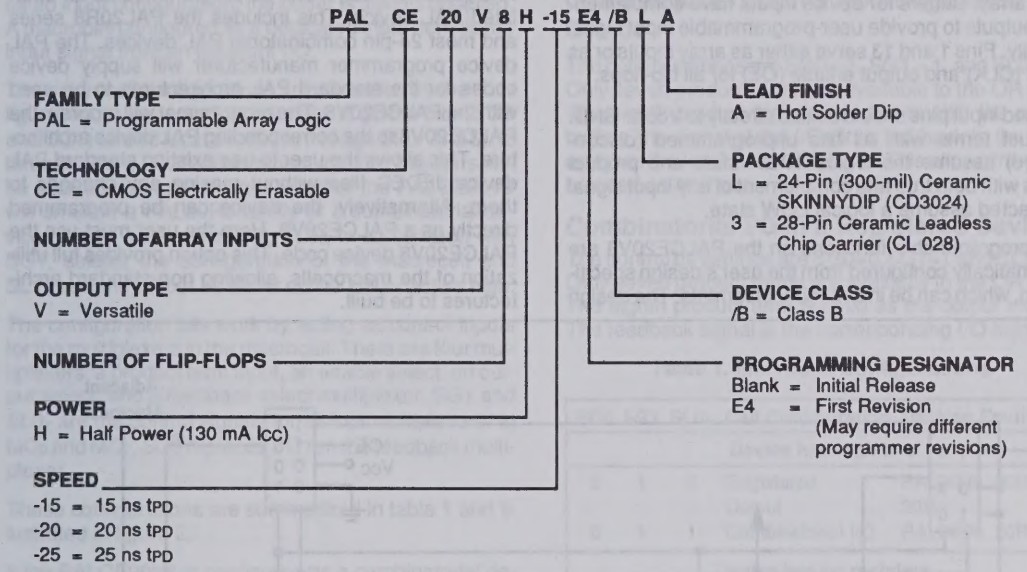
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE20V8H-15	E4	/BLA, /B3A
PALCE20V8H-20	Blank, E4	
PALCE20V8H-25		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

Group A Tests

Group A tests consist of subgroups 1, 2, 3, 7, 8, 9, 10 and 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

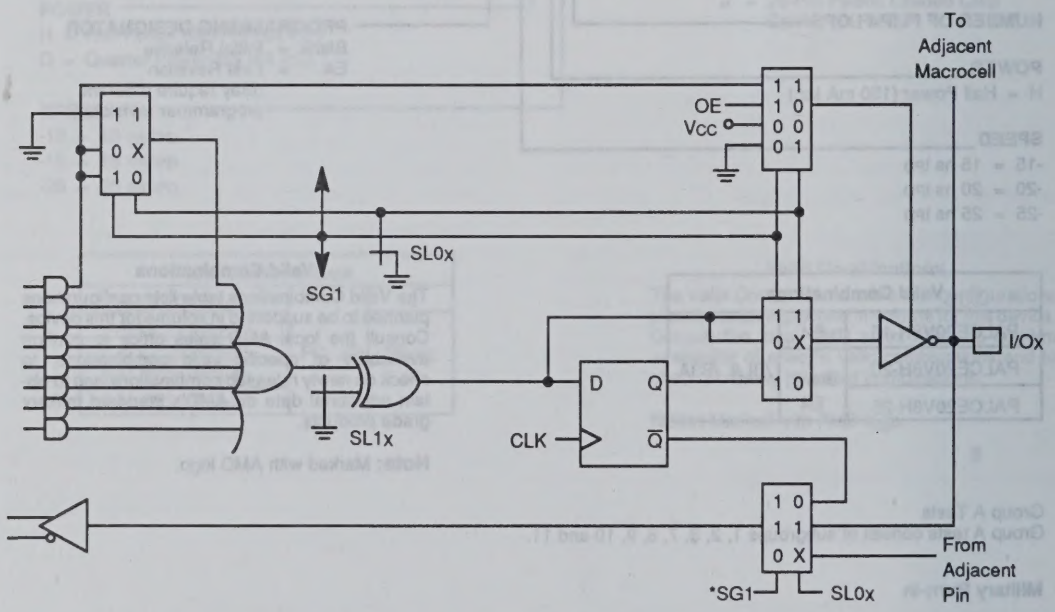
FUNCTIONAL DESCRIPTION

The PALCE20V8 is a universal PAL device. It has eight independently configurable macrocells ($MC_0..MC_7$). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 13 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$) for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE20V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE20V8. First, it can be programmed as an emulated PAL device. This includes the PAL20R8 series and most 24-pin combinatorial PAL devices. The PAL device programmer manufacturer will supply device codes for the standard PAL architectures to be used with the PALCE20V8. The programmer will program the PALCE20V8 to the corresponding PAL device architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed directly as a PALCE20V8. Here the user must use the PALCE20V8 device code. This option provides full utilization of the macrocells, allowing non-standard architectures to be built.



* In Macrocells MC_0 and MC_7, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.

Figure 1. PALCE20V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled. A macrocell configured as a dedicated input derives the input signal from an adjacent I/O.

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE20V8 will emulate a PAL20R8 family or a combinatorial device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell and $SL1_x$ sets the output as either active low or active high.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, $\overline{SG0}$ replaces SG1on the feedback multiplexer.

These configurations are summarized in table 1 and illustrated in figure 2.

If the PALCE20V8 is configured as a combinatorial device, the CLK and $\overline{OE}$ pins may be available as inputs to the array. If the device is configured with registers, the CLK and $\overline{OE}$ pins cannot be used as data inputs.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. $SL1_x$ is an input to the exclusive-OR gate which is the D input to the flip-flop. $SL1_x$ is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE20V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 0, and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 18(21) and 19(23). Pins 18(21) and 19(23) do not use feedback in this mode.

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. The feedback signal is an adjacent I/O pin.

Combinatorial I/O in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0,SG1=1 and $SL0_x$ =1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

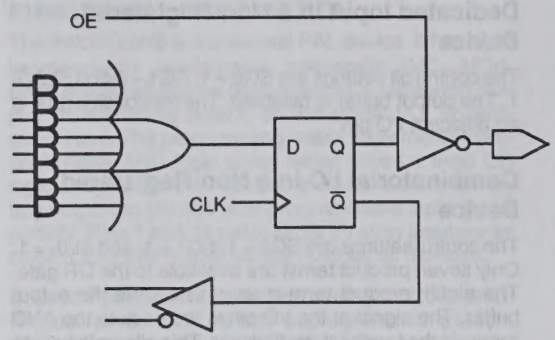
Table 1. Macrocell Configurations

SG0	SG1	$SL0_x$	Cell Configuration	Devices Emulated
Device has registers				
0	1	0	Registered Output	PAL20R8, 20R6, 20R4
0	1	1	Combinatorial I/O	PAL20R6, 20R4
Device has no registers				
1	0	0	Combinatorial Output	PAL20L2, 18L4,16L6,14L8
1	0	1	Dedicated Input	PAL20L2,18L4, 16L6
1	1	1	Combinatorial I/O	PAL20L8

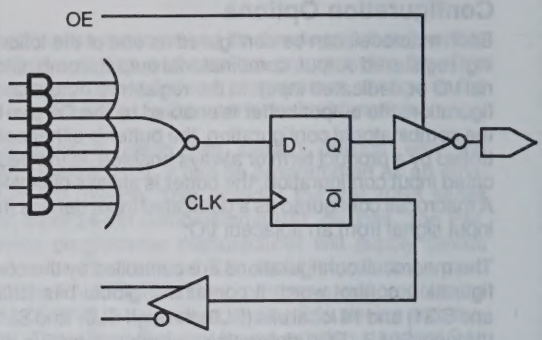
Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

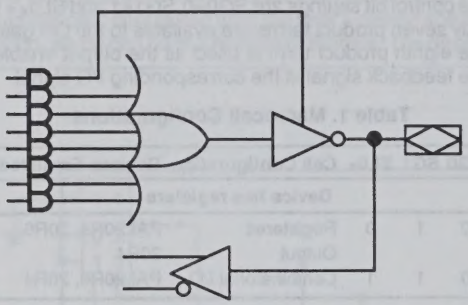
Selection is made through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is a 0 and active low if $SL1_x$ is a 1.



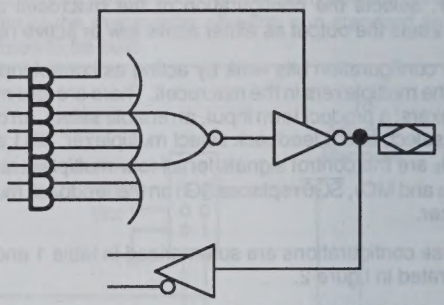
Registered Active Low



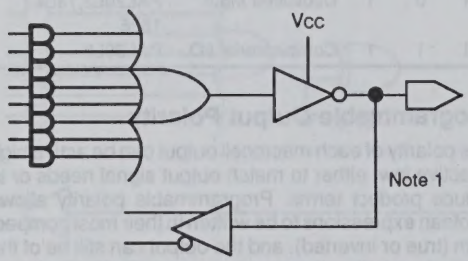
Registered Active High



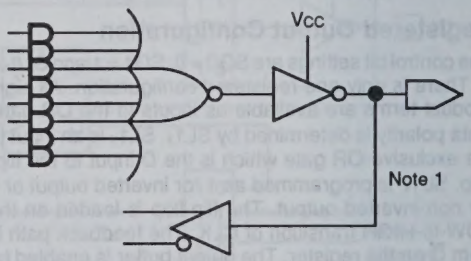
Combinatorial I/O Active Low



Combinatorial I/O Active High



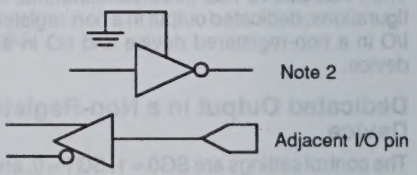
Combinatorial Output Active Low



Combinatorial Output Active High

Notes:

1. Feedback is not available on pins 18 (21) and 19 (23) in the combinatorial output mode.
2. This macrocell configuration is not available on pins 18 (21) and 19 (23).



Dedicated Input

12197-012C

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE20V8 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE20V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE20V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE20V8. It consists of 64 bits of programmable memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE20V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

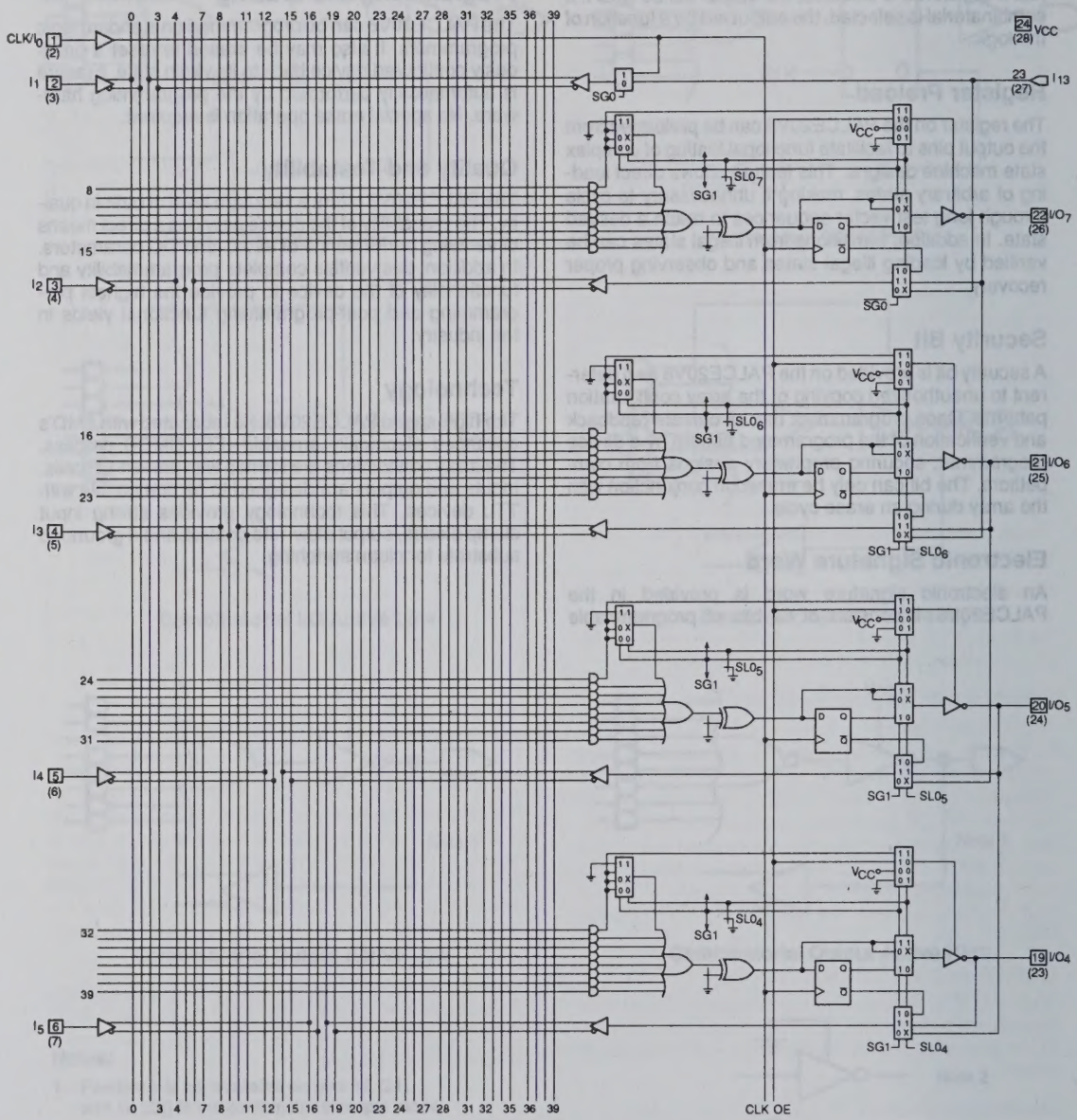
Quality and Testability

The PALCE20V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming and post-programming functional yields in the industry.

Technology

The high-speed PALCE20V8H is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP (PLCC and LCC) Pinouts



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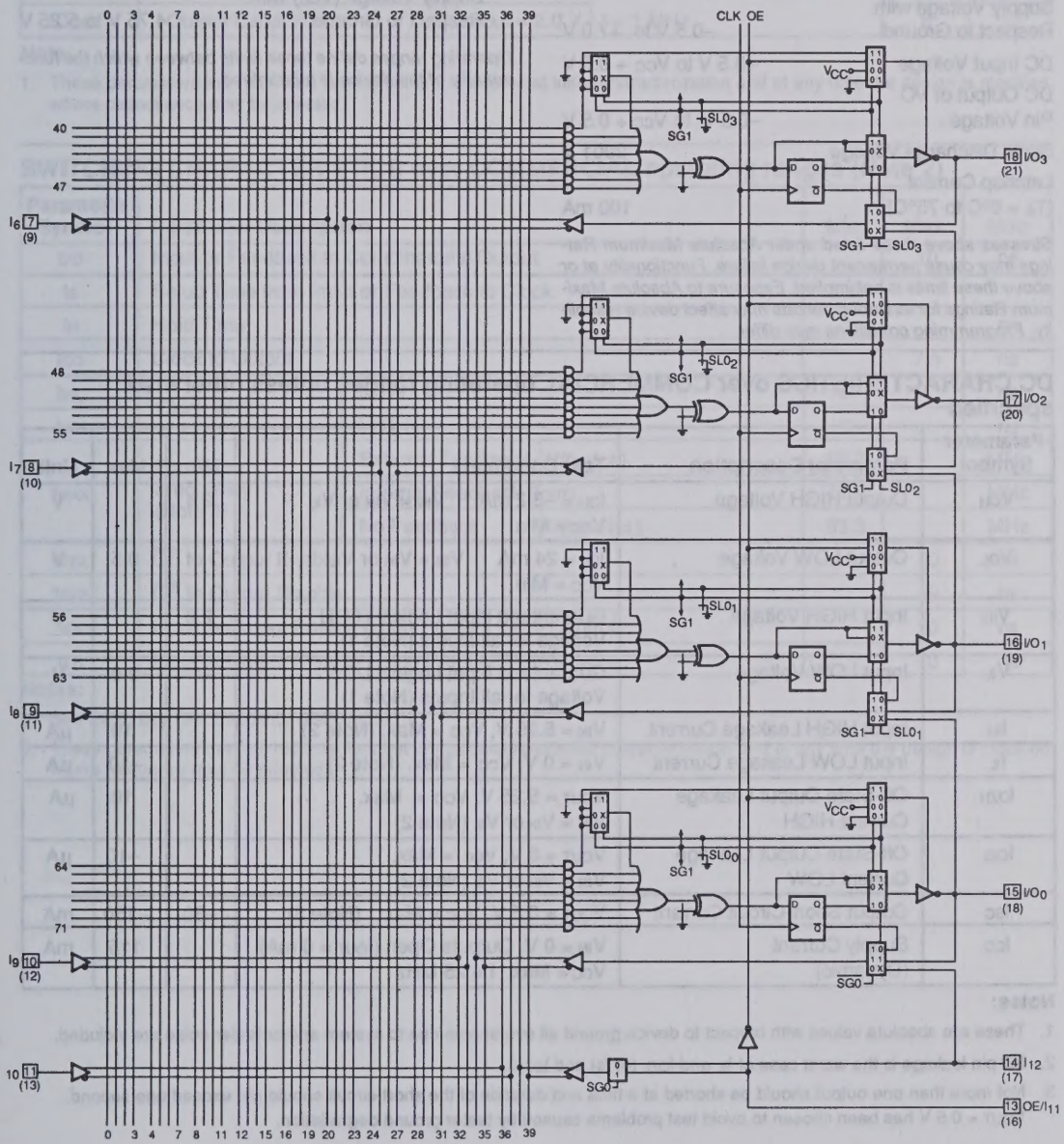
LOGIC DIAGRAM (Continued)
SKINNYDIP (PLCC and LCC) Pinouts



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concluded

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to 75°C
Supply Voltage (V_{CC}) with Respect to Ground	4.75 V to 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz		115	mA

Notes:

1. These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input or Feedback to Clock			7.5		
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				7.5	ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	66.7		MHz
		Internal Feedback (f_{CNT})		71.4		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				10	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				10	ns
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 15 MHz	H		90	mA
			Q		55	

Notes:

1. These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			–15 Min.	–15 Max.	–25 Min.	–25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{WL}	Clock Width	LOW		8		12		ns
t_{WH}		HIGH		8		12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	45.5		37		MHz
		Internal Feedback (f_{CNT})		50		40		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	62.5		41.6		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 1.0 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 1.0 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5.0 V, T_A = 25°C (Note 5)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz		130	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input or Feedback to Clock			12		
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				12	ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	1/(ts+tco)	41.6		MHz
		Internal Feedback (f_{CNT})		45.5		MHz
		No Feedback	1/(t_{WH}+t_{WL})	50.0		MHz
t_{PZX}	$\overline{OE}$ to Output Enable				15	ns
t_{PXZ}	$\overline{OE}$ to Output Disable				15	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)				15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)				15	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5.0 V, T_A = 25°C (Note 5)	–30	–150	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 25 MHz		130	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

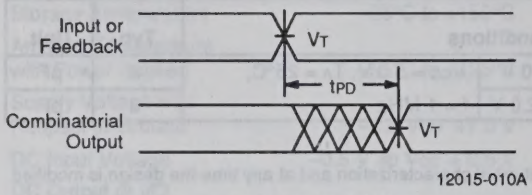
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			–20 Min.	–20 Max.	–25 Min.	–25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20		25	ns
t_S	Setup Time from Input or Feedback to Clock			15		20		ns
t_H	Hold Time (Note 5)			0		0		ns
t_{CO}	Clock to Output				15		20	ns
t_{WL}	Clock Width	LOW		12		15		ns
t_{WH}		HIGH		12		15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	33.3		25		MHz
		Internal Feedback (f_{CNT})		35.7		26.3		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	41.7		33.3		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				18		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				18		20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				20		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				20		25	ns

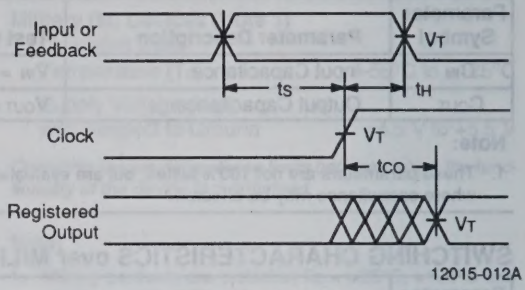
Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

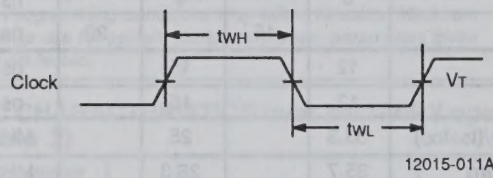
SWITCHING WAVEFORMS



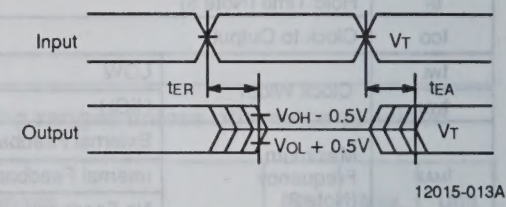
Combinatorial Output



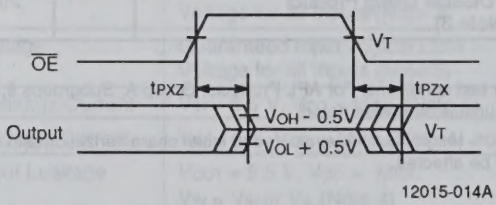
Registered Output



Clock Width



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable

Notes:

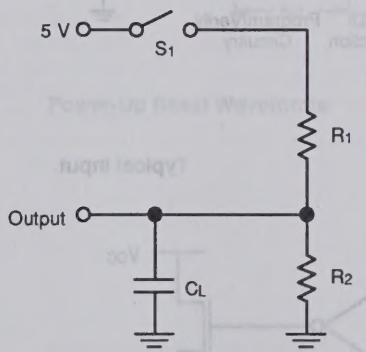
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12197-007A

Switching Test Circuit

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF	200 Ω	390 Ω	390 Ω	750 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

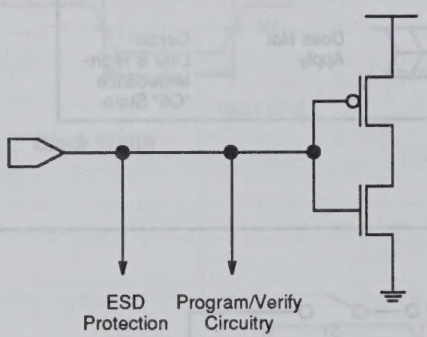
ENDURANCE CHARACTERISTICS

The PALCE20V8 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

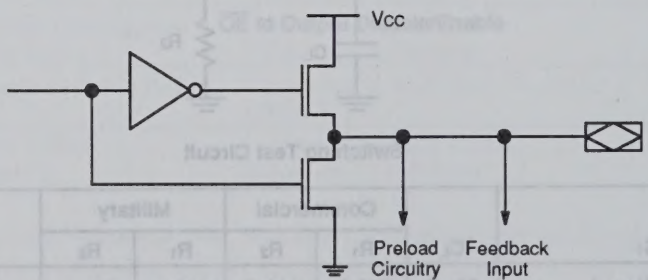
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

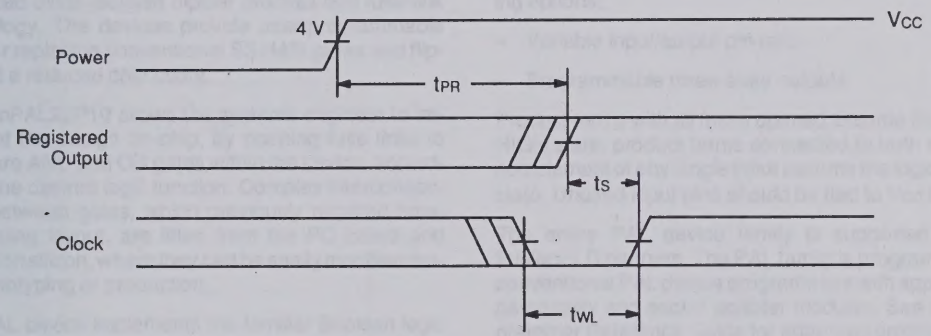
12197-013A

POWER-UP RESET

The PALCE20V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

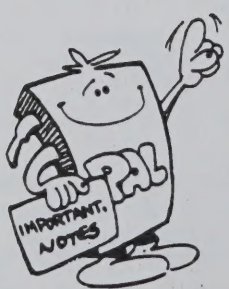
1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



12197-009A

Power-Up Reset Waveforms


IMPORTANT
NOTES

AmPAL22P10B/AL/A

24-Pin Combinatorial TTL Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 15 ns maximum propagation delay
- Universal combinatorial architecture
- Programmable output polarity
- Programmable replacement for high-speed TTL logic
- Extensive third–party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP and 28-pin PLCC packages save space

GENERAL DESCRIPTION

The AmPAL22P10 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The AmPAL22P10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

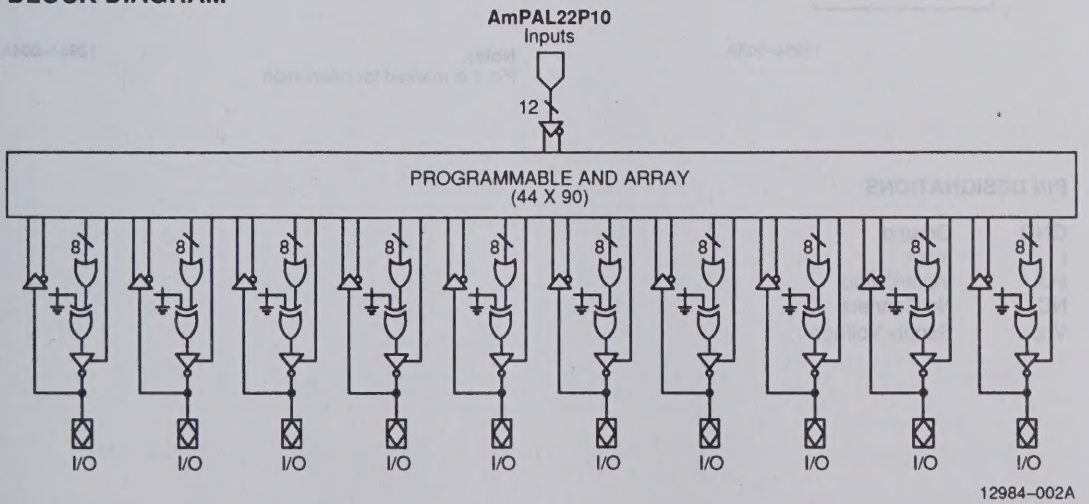
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs. In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Unused input pins should be tied to V_{CC} or GND.

The entire PAL device family is supported by the FusionPLD partners. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional fuse may be opened to prevent pattern readout. This feature secures proprietary circuits.

BLOCK DIAGRAM

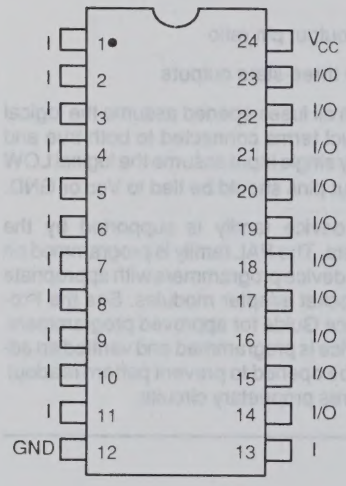


PRODUCT SELECTOR GUIDE

Family	t_{PD} ns (Max.)	I_{CC} mA (Max.)	I_{OL} mA (Min.)
Very High Speed ("B") Versions	15	210	24
High Speed ("A") Versions	25	210	24
High Speed, Half Power ("AL") Versions	25	105	24

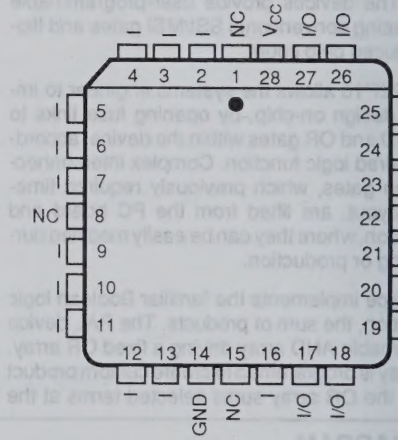
CONNECTION DIAGRAMS
Top View

SKINNYDIP



12984–003A

PLCC



Note:
Pin 1 is marked for orientation

12984–004A

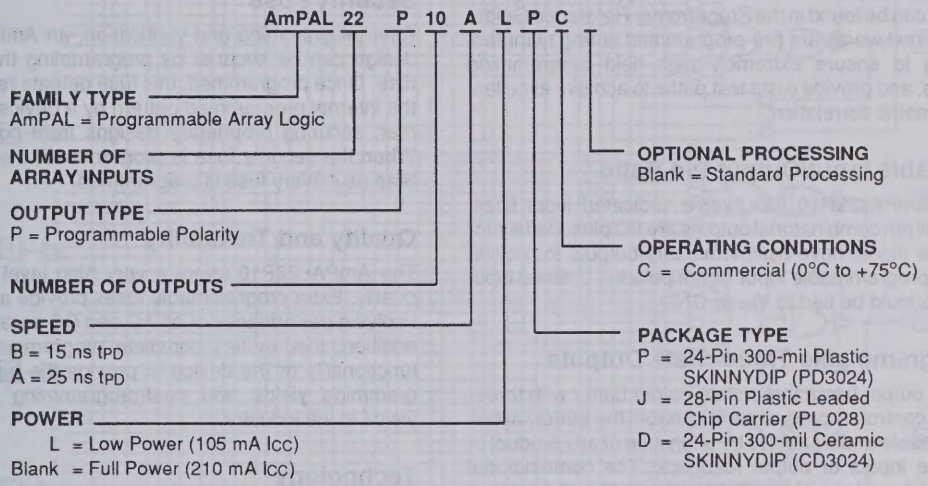
PIN DESIGNATIONS

GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
V_{CC}	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
AmPAL22P10	B, AL, A	PC, JC, DC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The AmPAL22P10 has twelve dedicated input lines, and all ten combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Polarity

The polarity of each output can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts. Selection is through a programmable fuse which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if the fuse is 1 (programmed) and active low if the fuse is 0 (intact).

Security Fuse

After programming and verification, an AmPAL22P10 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

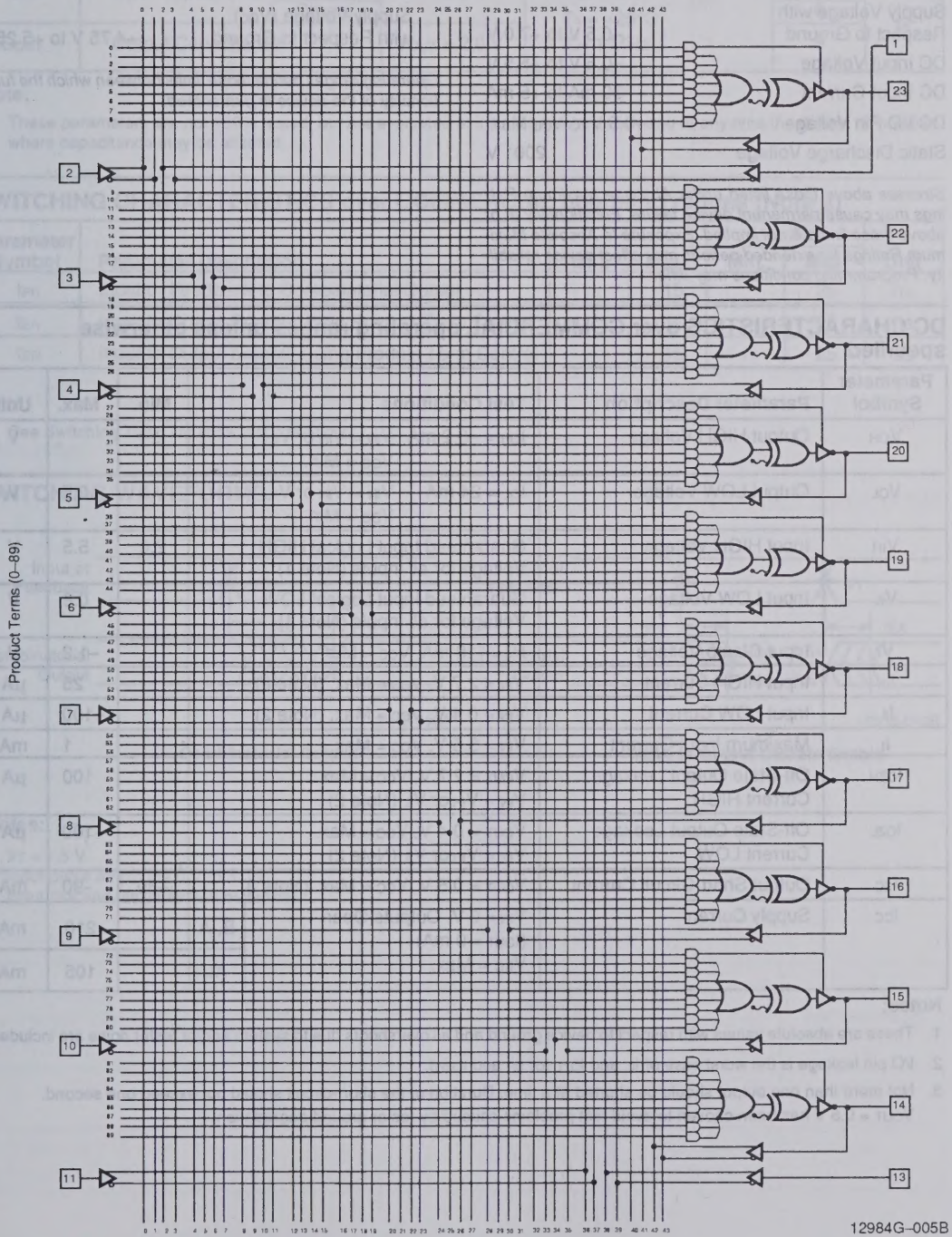
The AmPAL22P10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The AmPAL22P10 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for reliable operation.

LOGIC DIAGRAM

AmPAL22P10



12984G–005B

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature With Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to +5.5 V
DC Input Current	−30 mA to +5 mA
DC I/O Pin Voltage	−0.5 V to V_{CC} Max.
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.			−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			−100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		−30	−90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.	B, A		210	mA
			AL		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V	11	pF
		Others		T_A = +25°C	6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V	f = 1 MHz	9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

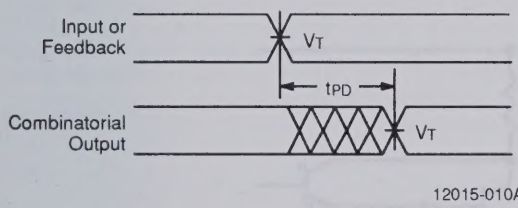
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	B		A, AL		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output		15		25	ns
t_{EA}	Input to Output Enable Using Product Term Control		18		25	ns
t_{ER}	Input to Output Disable Using Product Term Control		15		25	ns

Note:

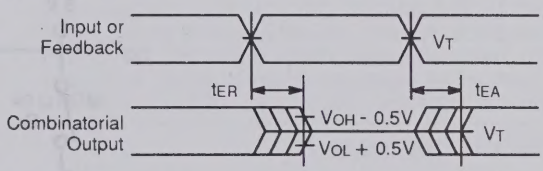
2. See Switching Test Circuit for test conditions.

SWITCHING WAVEFORMS



12015-010A

Combinatorial Output



12015-013B

Input to Output Disable/Enable

Notes:

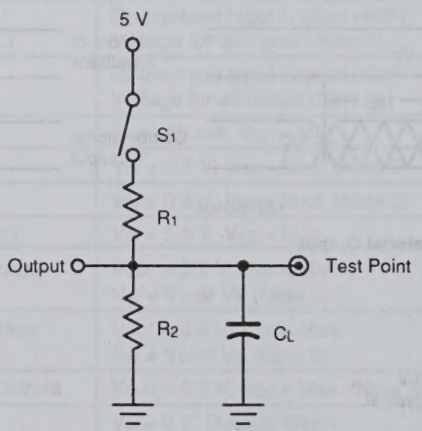
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

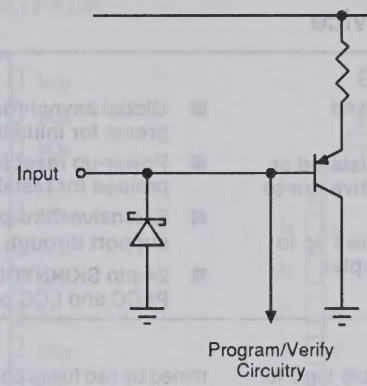


12350-019A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

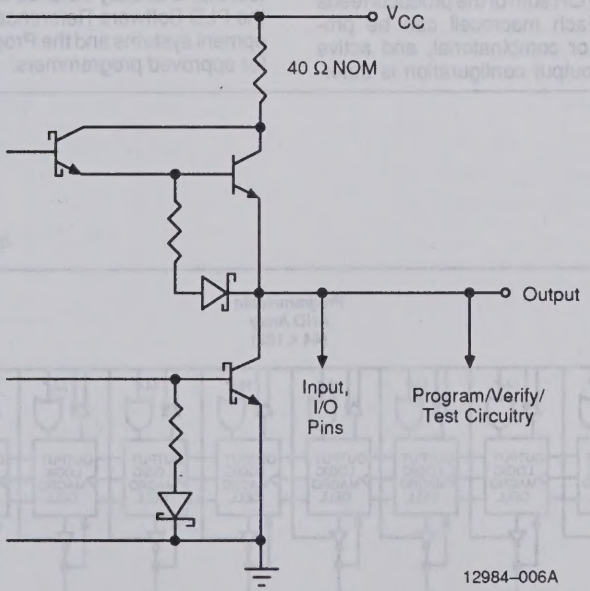
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



12350–020B

Typical Output



12984–006A

PAL22V10 Family, AmPAL22V10/A

24-Pin TTL Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 7.5 ns propagation delay and 91 MHz f_{MAX}
- 10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP, 24-pin Flatpack and 28-pin PLCC and LCC packages save space

GENERAL DESCRIPTION

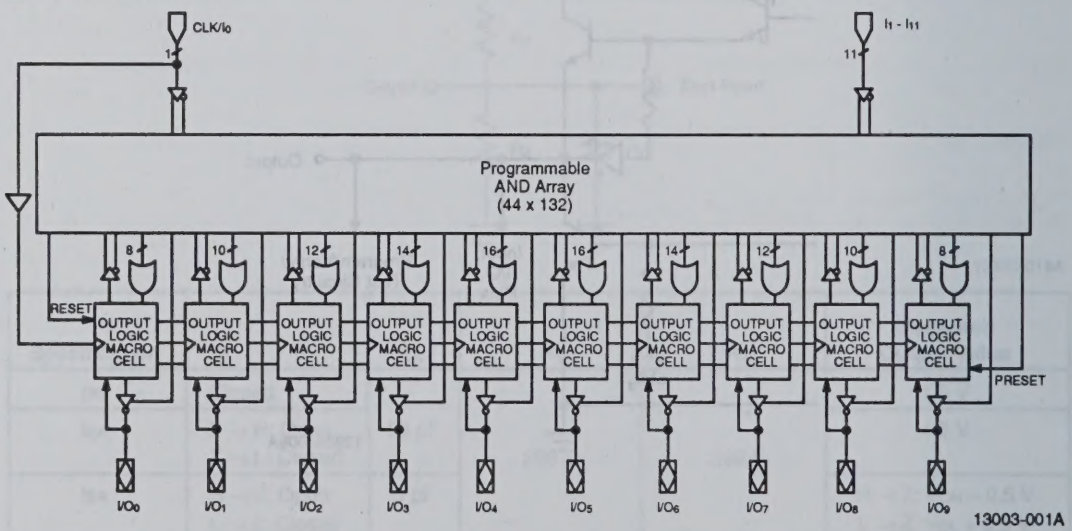
The PAL22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL22V10 device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two fuses controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PAL22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

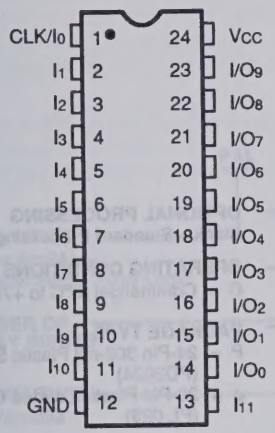
BLOCK DIAGRAM



Publication# 16559 Rev. A Amendment/0
Issue Date: January 1992

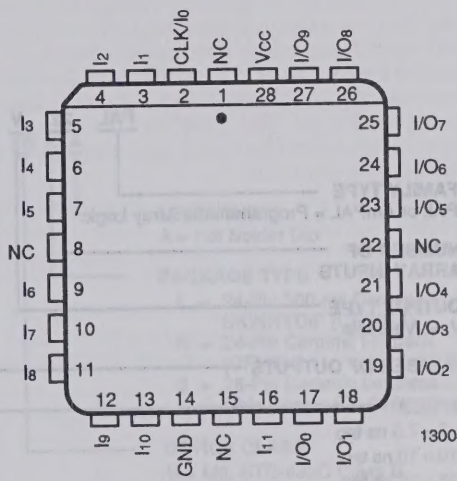
CONNECTION DIAGRAMS
Top View

SKINNYDIP/FLATPACK



13003-002A

PLCC/LCC



13003-003A

Note:
Pin 1 is marked for orientation.

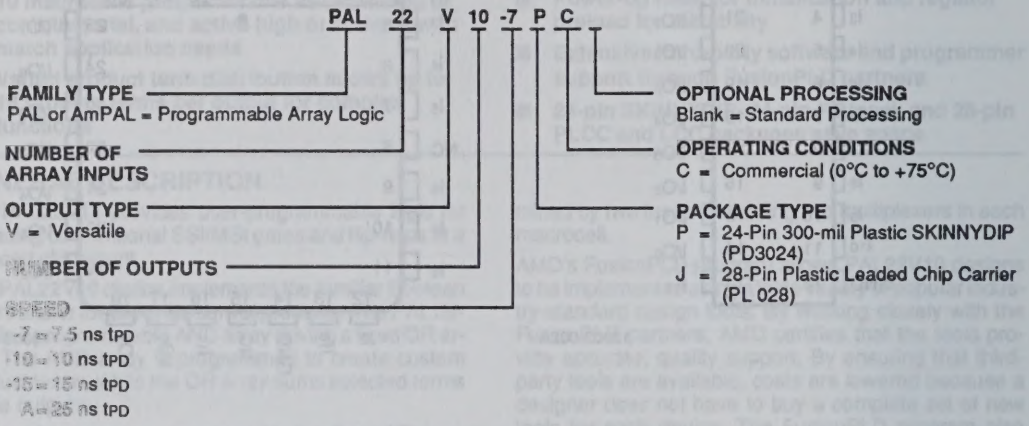
PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
Vcc	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL22V10-7	PC, JC
PAL22V10-10	
PAL22V10-15	
AmPAL22V10A	

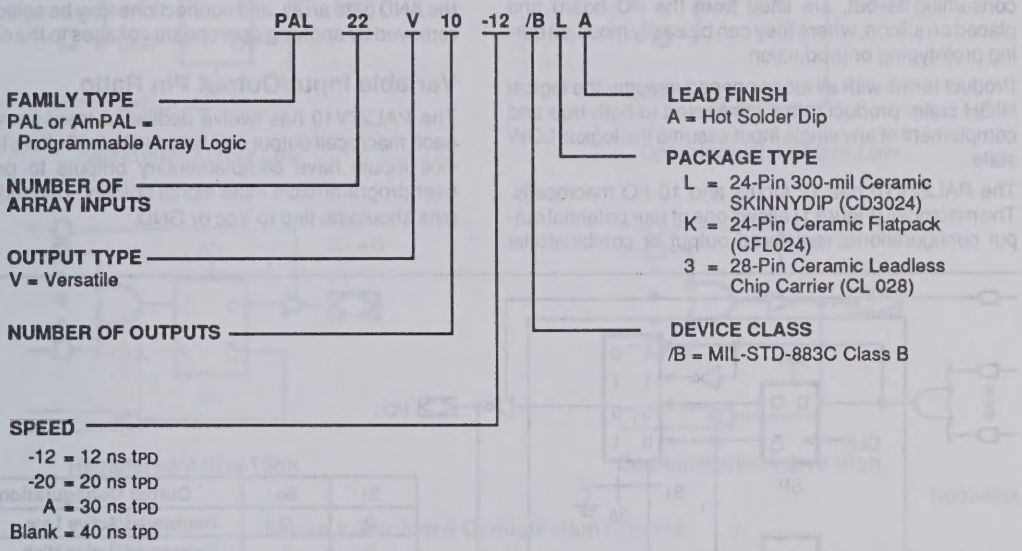
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PAL22V10-12	/BLA, /BKA, /B3A
PAL22V10-20	
AmPAL22V10A	
AmPAL22V10	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PAL22V10 utilizes Advanced Micro Devices' advanced oxide-isolated bipolar process and fuse-link technology. The device provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

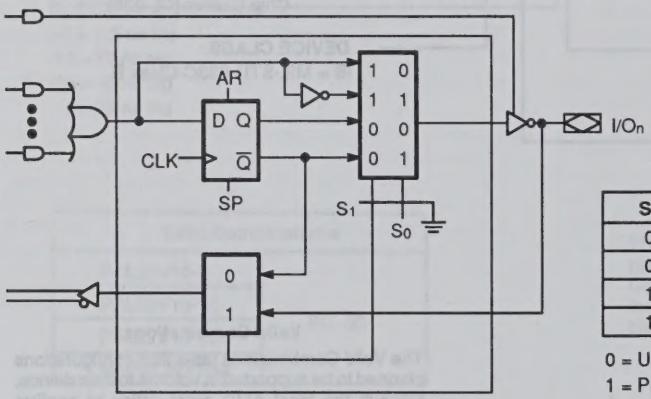
Product terms with all fuses opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PAL22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls initially are connected to ground (0) through a programmable fuse, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit.

Variable Input/Output Pin Ratio

The PAL22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Unprogrammed fuse
1 = Programmed fuse

13003-004A

Figure 1. Output Logic Macrocell Diagram

Registered Output Configuration

Each macrocell of the PAL22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.

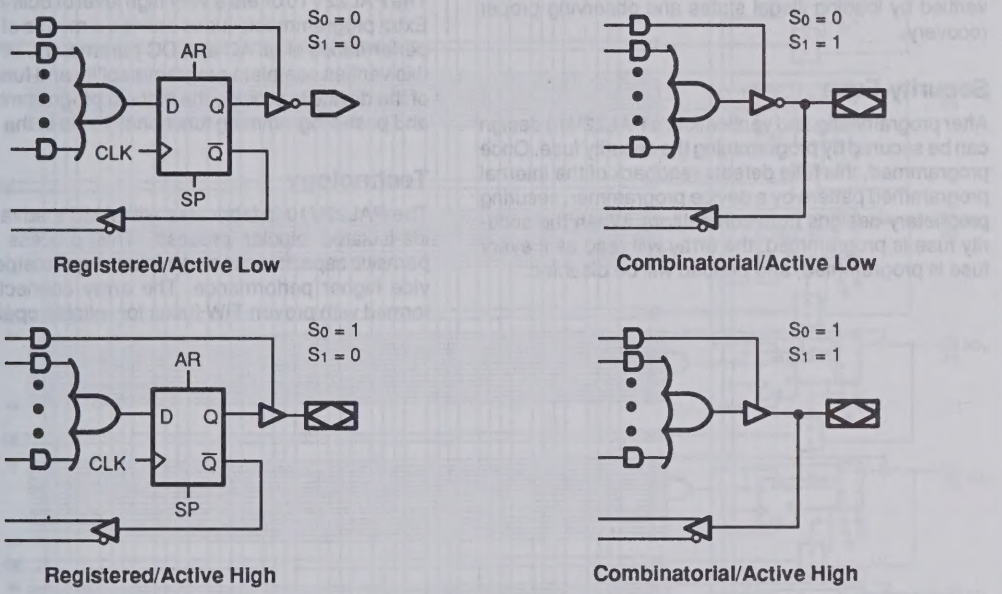


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions.

Preset/Reset

For initialization, the PAL22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PAL22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL22V10 design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed, and preload will be disabled.

Programming

The PAL22V10 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

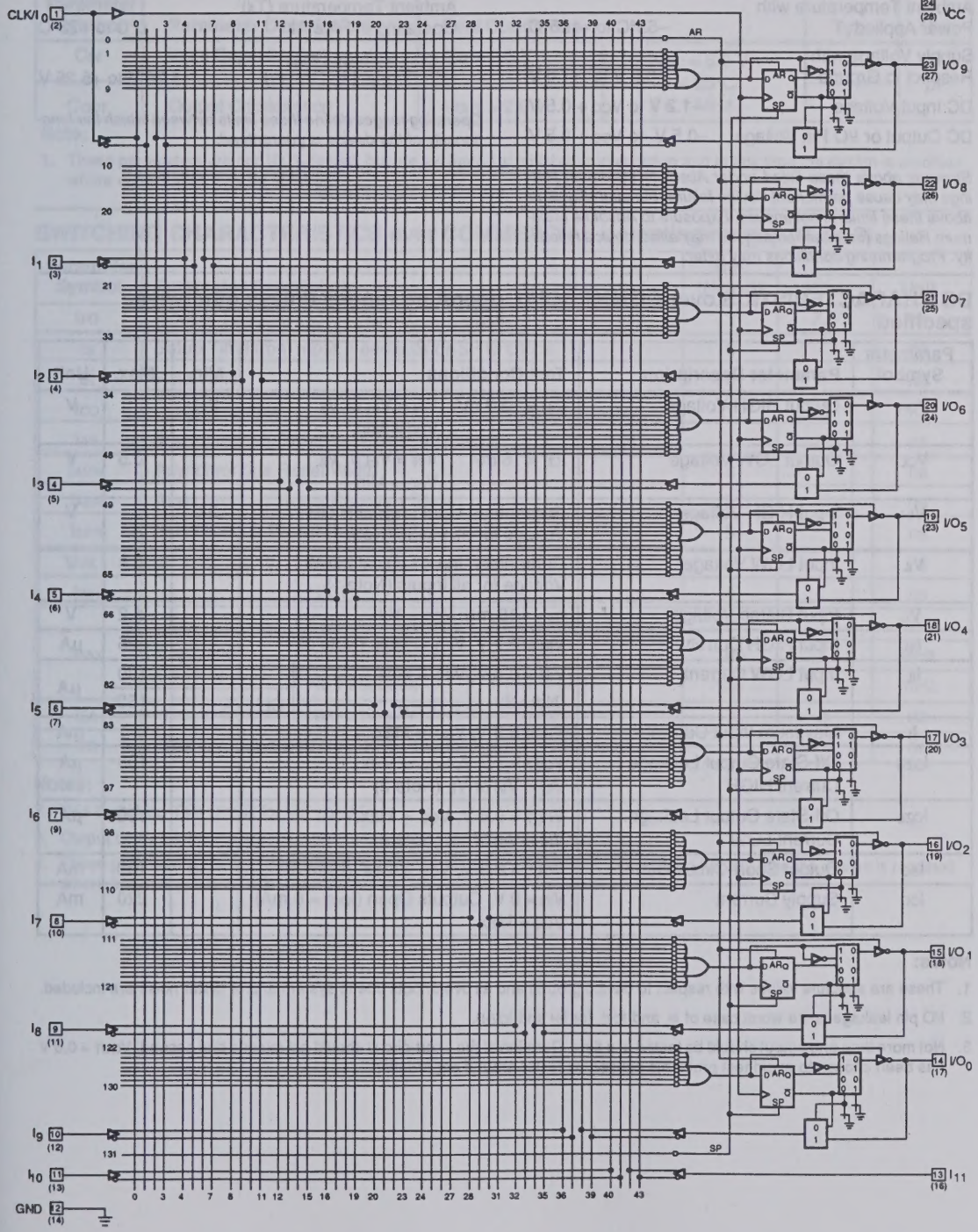
Quality and Testability

The PAL22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The PAL22V10 is fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven TiW fuses for reliable operation.

LOGIC DIAGRAM
SKINNYDIP (PLCC/LCC) Pinouts



13003-006A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)			–100	µA
			CLK		–150	
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			220	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		5	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	7.5	ns
t_S	Setup Time from Input, Feedback or SP to Clock			5		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	6	ns
t_{AR}	Asynchronous Reset to Registered Output				12	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			5		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	91		MHz
		Internal Feedback (f_{CNT})		100		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				8	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.			–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)			25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max.			–100	µA
		(Note 2)	CLK		–150	
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.			1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		5	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	10	ns
t_S	Setup Time from Input, Feedback or SP to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output			1	7	ns
t_{AR}	Asynchronous Reset to Registered Output				15	ns
t_{ARW}	Asynchronous Reset Width			10		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		5		ns
t_{WH}		HIGH		5		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	71		MHz
		Internal Feedback (f_{CNT})		80		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	100		MHz
t_{EA}	Input to Output Enable Using Product Term Control				11	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Input Current	–30 mA to +5 mA
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		6	
				5	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min. (Note 3)	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width			15		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		ns
t_{SPR}	Synchronous Preset Recovery Time			10		ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})		80		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Output delay minimums are measured under best-case conditions.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Input Current	–30 mA to +5 mA
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	11	pF
				6	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			20		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				30	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			35		ns
t_{SPR}	Synchronous Preset Recovery Time			20		ns
t_{WL}	Clock Width	LOW		15		ns
t_{WH}		HIGH		15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	1/(ts + tco)	28.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.2 V to +7.0 V
DC Output or I/O Pin Voltage	–0.5 V to +7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–100	µA
		CLK		–150	
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				12	ns
t_S	Setup Time from Input or Feedback to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)			10		ns
t_{SPR}	Synchronous Preset Recovery Time (Note 4)			10		ns
t_{WL}	Clock Width	LOW		6		ns
t_{WH}		HIGH		6		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})		58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83.3		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)				15	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)				12.5	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_S and t_{AR}.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to +5.5 V
DC Output or I/O Pin Voltage	−0.5 V to +7.0 V
DC Input Current	−30 mA to +5 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	−55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = −18 mA, V_{CC} = Min.		−1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		−100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		200	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	9	pF
				6	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20	ns
t_S	Setup Time from Input or Feedback to Clock			17		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)			20		ns
t_{SPR}	Synchronous Preset Recovery Time (Note 4)			20		ns
t_{WL}	Clock Width	LOW		15		ns
t_{WH}		HIGH		15		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	31.2		MHz
		Internal Feedback (f_{CNT})		33.3		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 4)				20	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 4)				20	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of t_S and t_{AR}.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} Max.
DC Input Current	–30 mA to +5 mA
Output Sink Current	100 mA (Note 6)

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Ambient Temperature (T_A) Operating in Free Air	–55°C Min.
Operating Case (T_C) Temperature	125°C Max.
Supply Voltage (V_{CC}) with Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C, and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V, V_{CC} = Max. (Note 4)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 4)		–100	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		1	mA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
6. Not more than one output should sink 100 mA at a time. Duration should not exceed one second.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description		Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	Pins 1, 13	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	11	pF
		Others			6	
C_{OUT}	Output Capacitance		V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

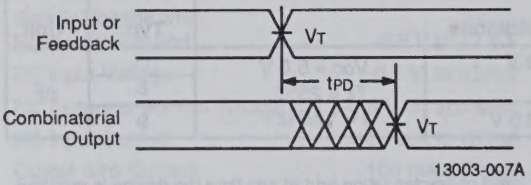
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			A		Std		Unit
				Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output				30		40	ns
t_S	Setup Time from Input or Feedback to Clock			25		35		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				20		25	ns
t_{AR}	Asynchronous Reset to Registered Output				35		45	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			30		40		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)			30		40		ns
t_{WL}	Clock Width	LOW		20		30		ns
t_{WH}		HIGH		20		30		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(ts + tco)	22		16.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 5)				30		40	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 5)				30		40	ns

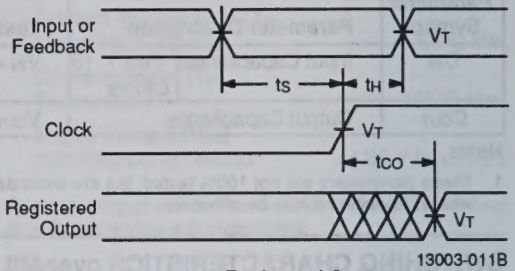
Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. t_{ARW} and t_{ARR} are not directly tested, but are guaranteed by the testing of ts and t_{AR}.
4. These parameters are not 100% tested, but are calculated at initial charzation ond at any time the design is modified where frequency may be affected.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

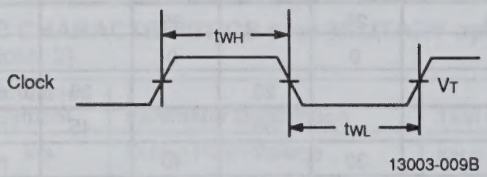
SWITCHING WAVEFORMS



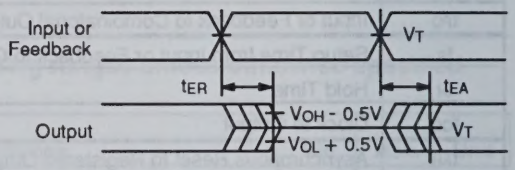
Combinatorial Output



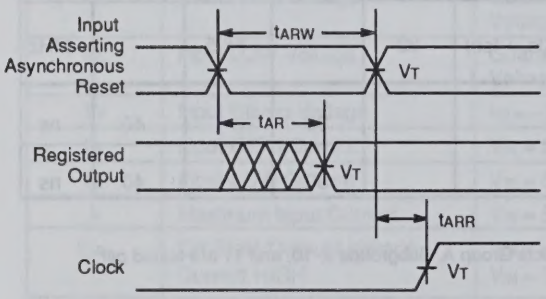
Registered Output



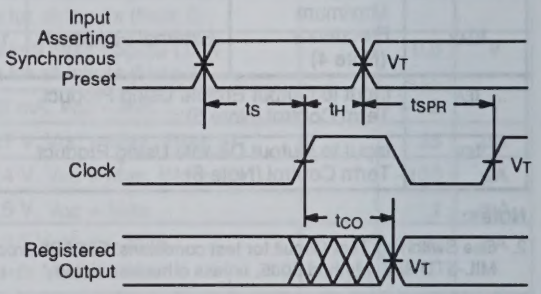
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

Notes:

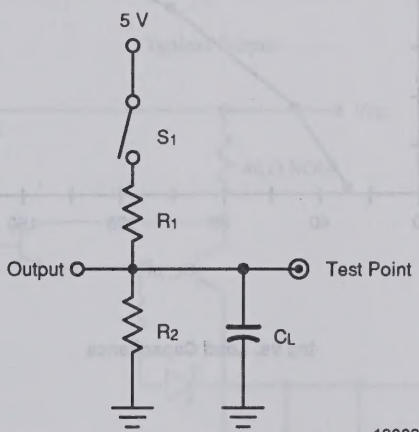
1. V_T = 1.5 V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–4 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

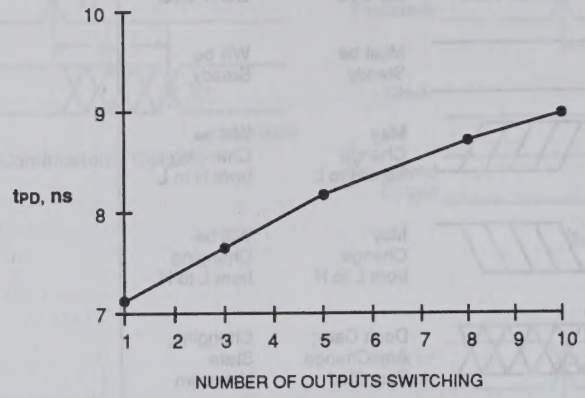


13003-015A

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Military R_1	Military R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

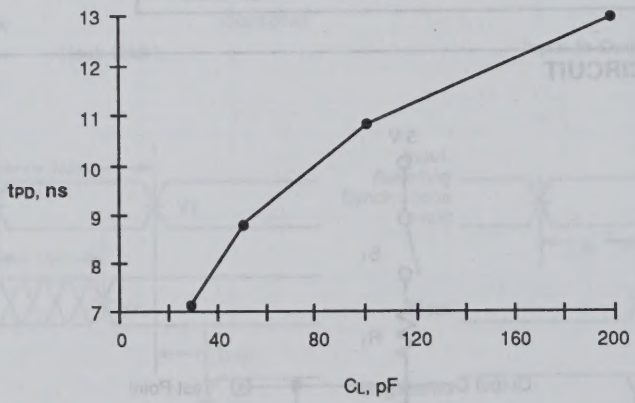
MEASURED SWITCHING CHARACTERISTICS for the PAL22V10-10

V_{CC} = 4.75 V, T_A = 75°C (Note 1)



t_{PD} vs. Number of Outputs Switching

13003-016A



t_{PD} vs. Load Capacitance

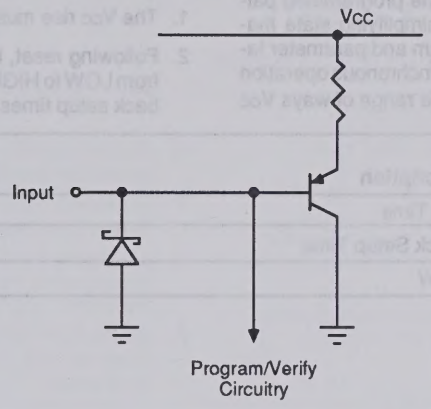
13003-017A

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where t_{PD} may be affected.

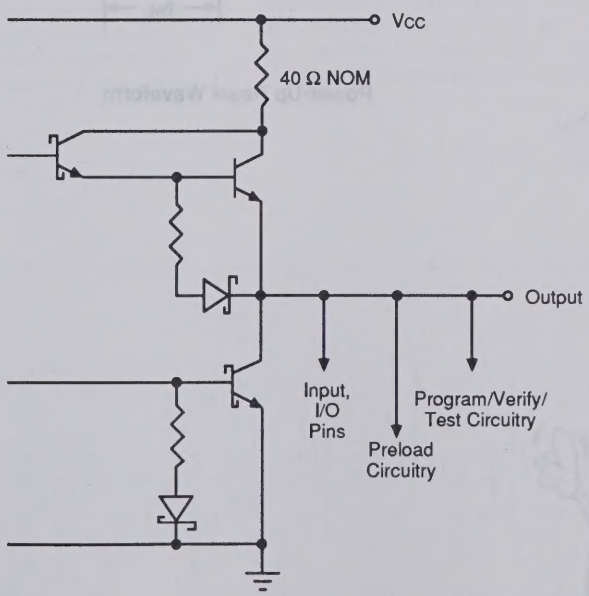
INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



13003-019A

Typical Output



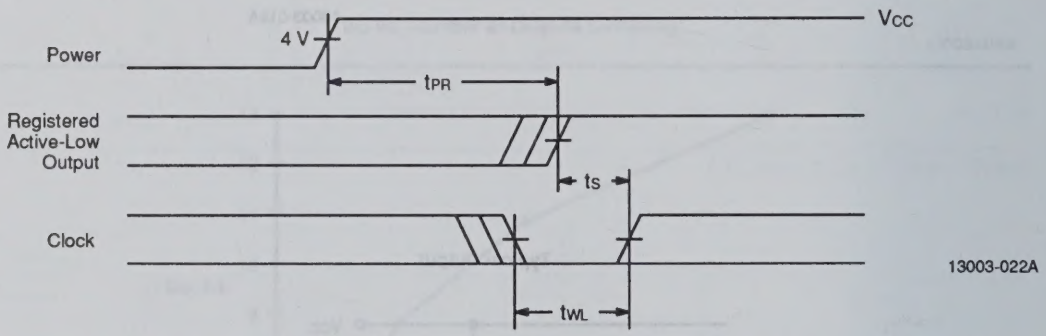
13003-020A

POWER-UP RESET

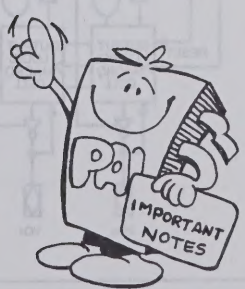
The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform


IMPORTANT
NOTES

Advanced Micro Devices

PALCE22V10 Family

24-Pin EE CMOS Versatile PAL Device

DISTINCTIVE CHARACTERISTICS

- As fast as 10 ns propagation delay and 83.3 MHz f_{MAX}
- Low-power EE CMOS
- 10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP, 24-pin SOIC, 24-pin Flatpack and 28-pin PLCC and LCC packages save space

GENERAL DESCRIPTION

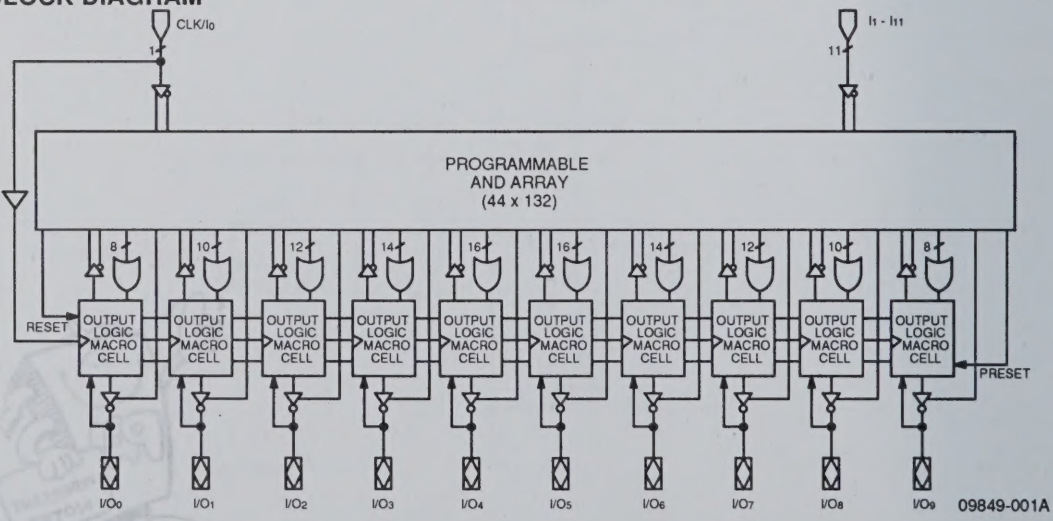
The PALCE22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

BLOCK DIAGRAM

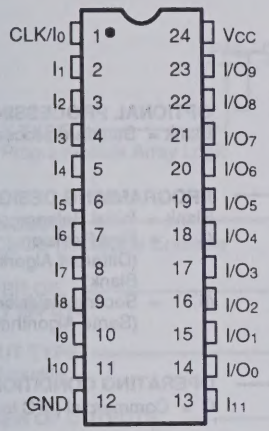


Publication# 16564 Rev. A Amendment/0
Issue Date: January 1992

CONNECTION DIAGRAMS

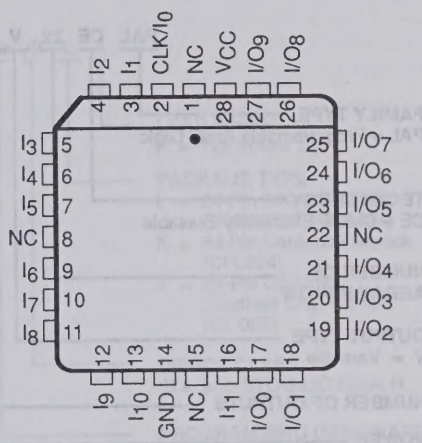
Top View

SKINNYDIP/SOIC/FLATPACK



09849-002A

PLCC/LCC



09849-003A

Note:
Pin 1 is marked for orientation.

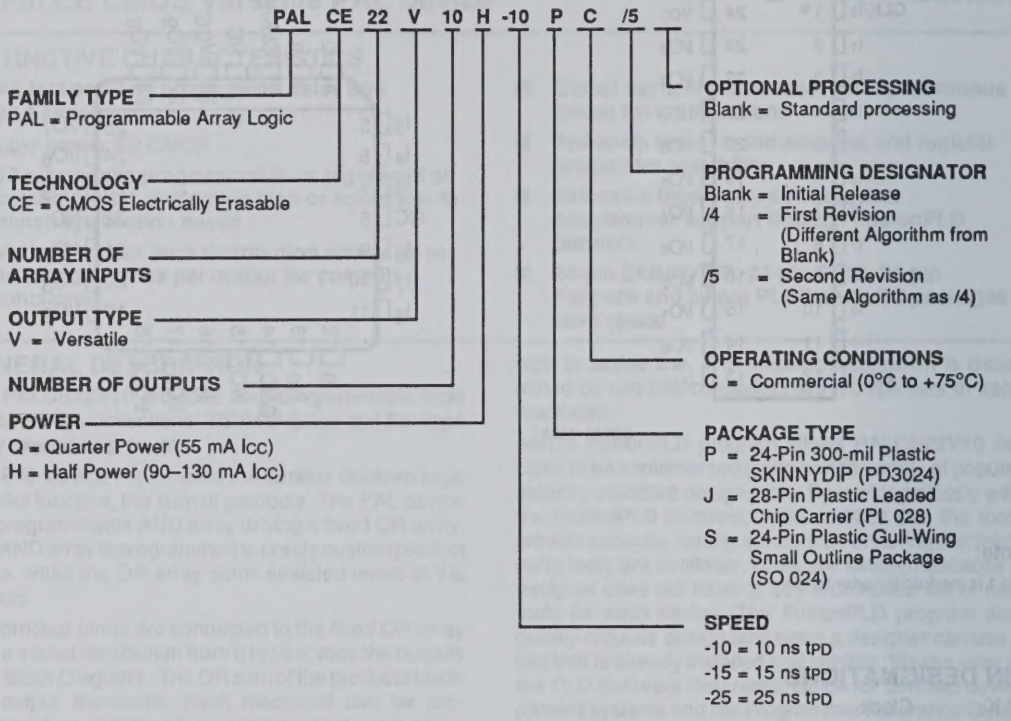
PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
Vcc	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE22V10H-10	PC, JC	/5
PALCE22V10H-15		/4, /5
PALCE22V10H-25	PC, JC, SC	Blank, /4
PALCE22V10Q-25		
PALCE22V10H-15		
PALCE22V10H-25		

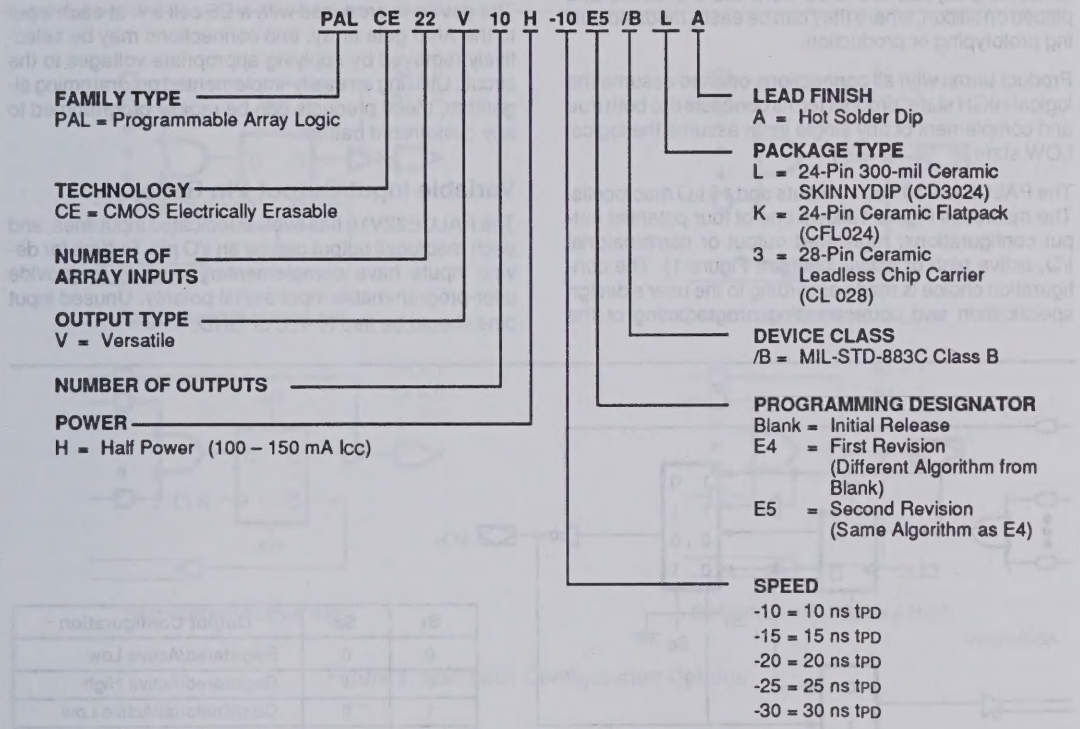
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE22V10H-10	E5	/BLA, /BKA, /B3A
PALCE22V10H-15	E4, E5	
PALCE22V10H-20	Blank, E4	
PALCE22V10H-25		
PALCE22V10H-30		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PALCE22V10 allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

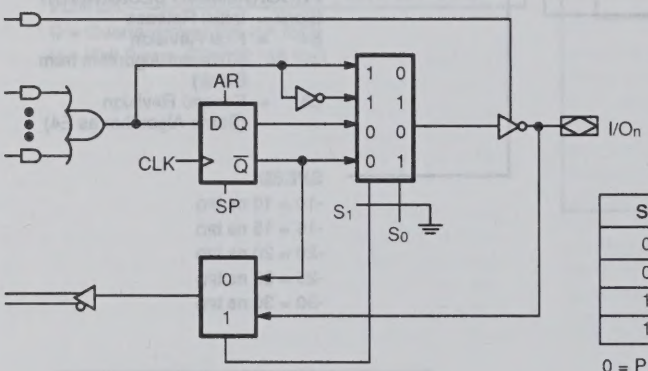
Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10 has 12 inputs and 10 I/O macrocells. The macrocell Figure 1allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 1). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 - S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

The PALCE22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

09849-004A

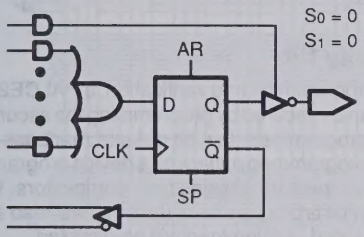
Figure 1. Output Logic Macrocell Diagram

Registered Output Configuration

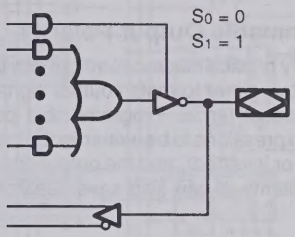
Each macrocell of the PALCE22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

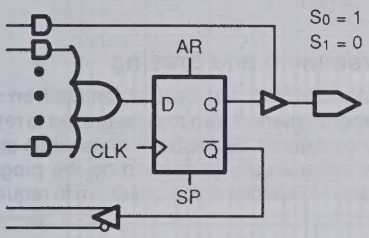
Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.



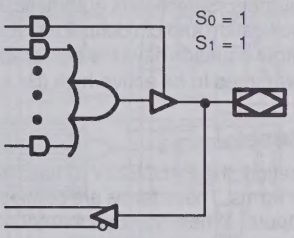
Registered/Active Low



Combinatorial/Active Low



Registered/Active High



Combinatorial/Active High

09849-005A

Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10 design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

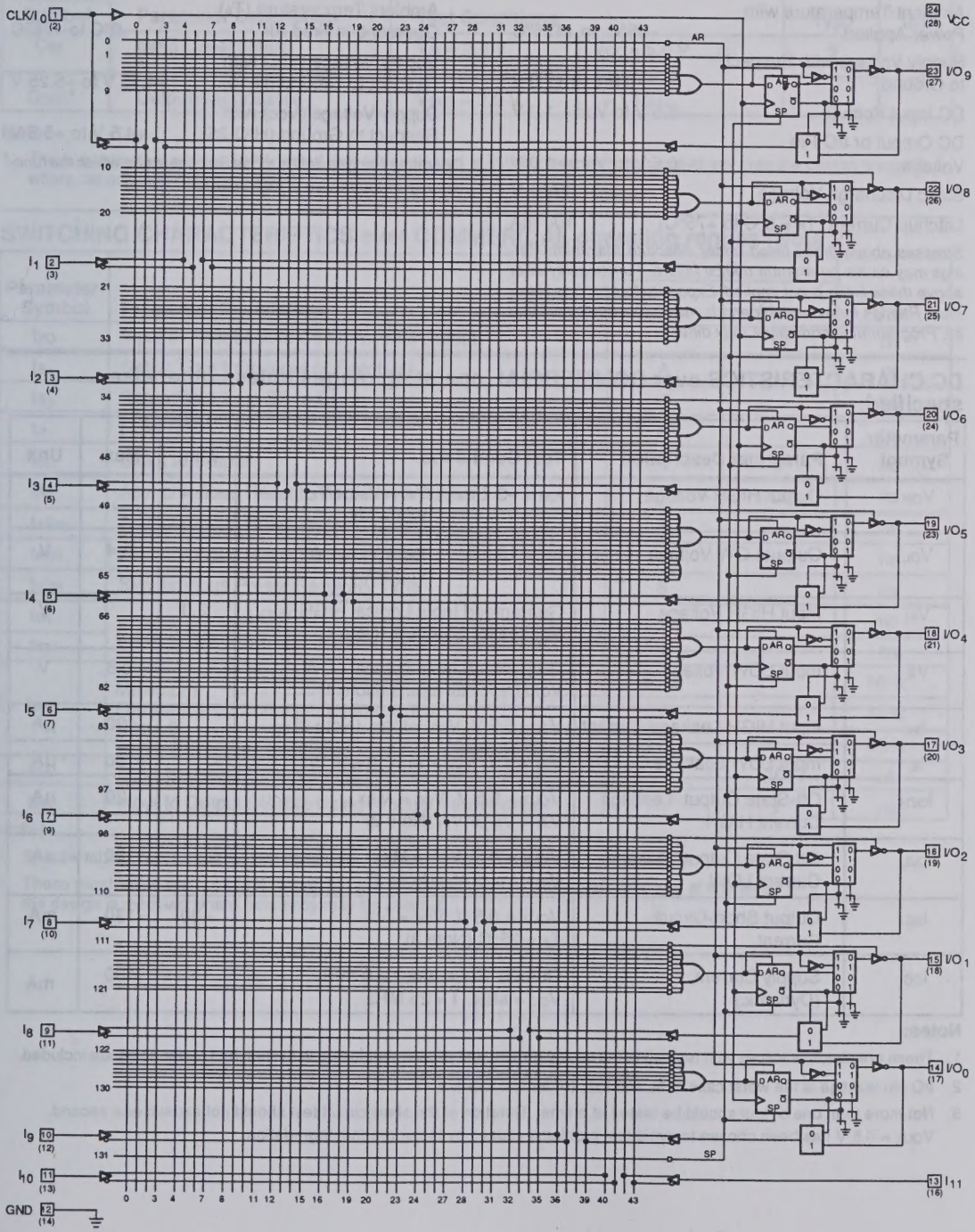
Quality and Testability

The PALCE22V10 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE22V10 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clear switching.

LOGIC DIAGRAM
SKINNYDIP/SOIC/FLATPACK (PLCC/LCC) Pinouts



09849-006A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 1.0 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 1.0 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground (H-15)	+4.75 V to +5.25 V
Supply Voltage (V_{CC}) with Respect to Ground (H/Q-25)	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)		20	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)		20	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)	−30	−130	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max., f = 25 MHz		130	mA

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10 Min.	-10 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_{S_1}	Setup Time from Input or Feedback			6		ns
t_{S_2}	Setup Time from SP to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{AR}	Asynchronous Reset to Registered Output				13	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	83.3		MHz
		Internal Feedback (f_{CNT})		110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground (H-15)	+4.75 V to +5.25 V
Supply Voltage (V_{CC}) with Respect to Ground (H/Q-25)	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.	H		90	mA
			Q		55	

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		15	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		25		ns
t_{SPR}	Synchronous Preset Recovery Time			10		25		ns
t_{WL}	Clock Width	LOW		8		13		ns
t_{WH}		HIGH		8		13		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		33.3		MHz
		Internal Feedback (f_{CNT})		58.8		35.7		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 1.0 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 1.0 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = –55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		20	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 4)		20	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} (Note 4)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 5)	–50	–135	mA
I_{CC}	Supply Current (Dynamic)	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max., f = 25 MHz		150	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

PRELIMINARY

Symbol	Parameter Description			–10 Min.	–10 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_{S_1}	Setup Time from Input or Feedback			8		ns
t_{S_2}	Setup Time from SP to Clock			10		ns
t_H	Hold Time (Note 3)			0		ns
t_{CO}	Clock to Output				8	ns
t_{AR}	Asynchronous Reset to Registered Output				15	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			10		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)			10		ns
t_{SPR}	Synchronous Preset Recovery Time			10		ns
t_{WL}	Clock Width	LOW		5		ns
t_{WH}		HIGH		5		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	62.5		MHz
		Internal Feedback (f_{CNT})		87		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	100		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				10	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				10	ns

Notes:

2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 7, 8, 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 1.0 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = –55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} (Note 4)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 5)		–50	–135	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max.	-15/-20		120	mA
			-25/-30		100	

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		9	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

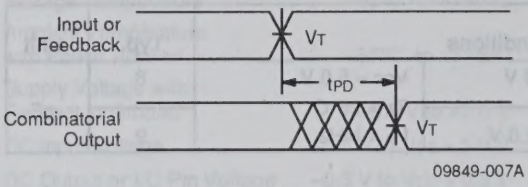
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		-15		-20		-25		-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output			15		20		25		30	ns
t_S	Setup Time from Input, Feedback or SP to Clock		12		15		18		20		ns
t_H	Hold Time (Note 3)		0		0		0		0		ns
t_{CO}	Clock to Output			8		15		20		20	ns
t_{AR}	Asynchronous Reset to Registered Output			20		25		25		30	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		25		30		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		15		20		25		30		ns
t_{SPR}	Synchronous Preset Recovery Time		15		20		25		30		ns
t_{WL}	Clock Width	LOW	8		10		15		15		ns
t_{WH}		HIGH	8		10		15		15		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback 1/(ts + tco)	50		33.3		26.3		25		MHz
		Internal Feedback (f_{CNT})	53		40		32.2		25		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)			15		20		25		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)			15		20		25		25	ns

Notes:

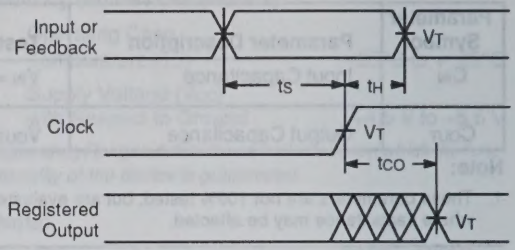
2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 7, 8, 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

SWITCHING WAVEFORMS



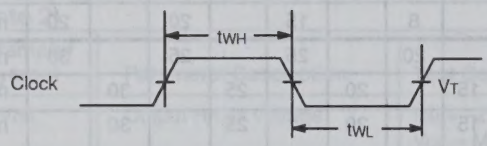
09849-007A

Combinatorial Output



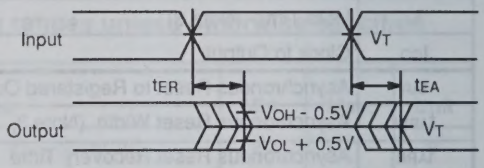
09849-008B

Registered Output



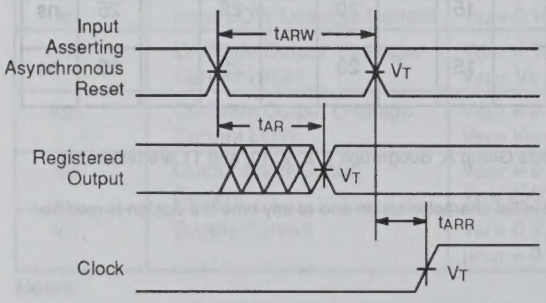
09849-011B

Clock Width



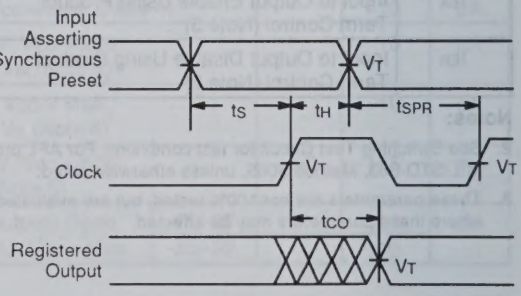
09849-012B

Input to Output Disable/Enable



09849-013B

Asynchronous Reset



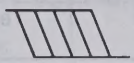
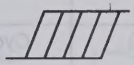
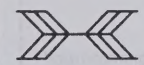
09849-014B

Synchronous Preset

Notes:

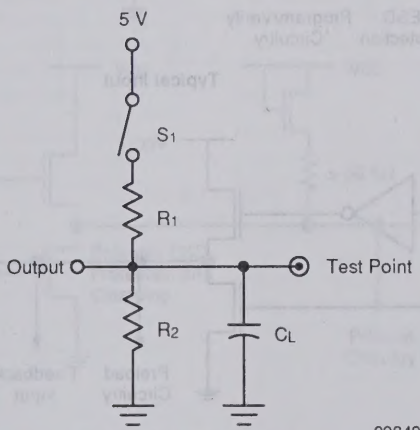
1. $V_T = 1.5$ V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	Must be Steady	Will be Steady
———		
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



09849-015A

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

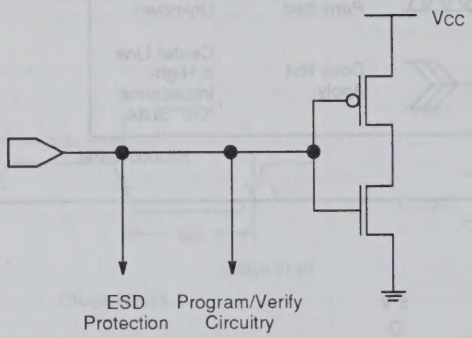
ENDURANCE CHARACTERISTICS

The PALCE22V10 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

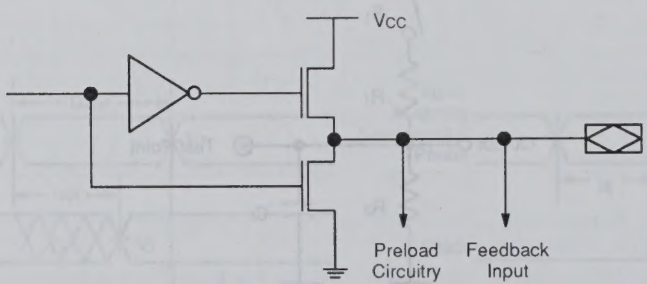
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



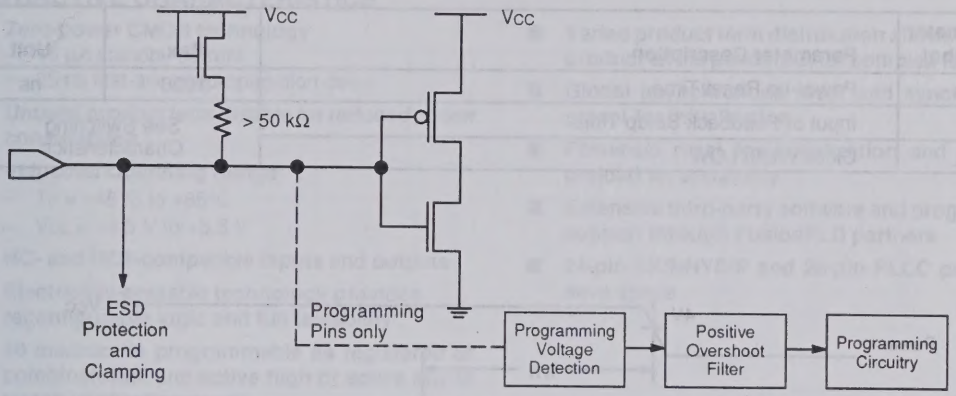
Typical Output

09849-017A

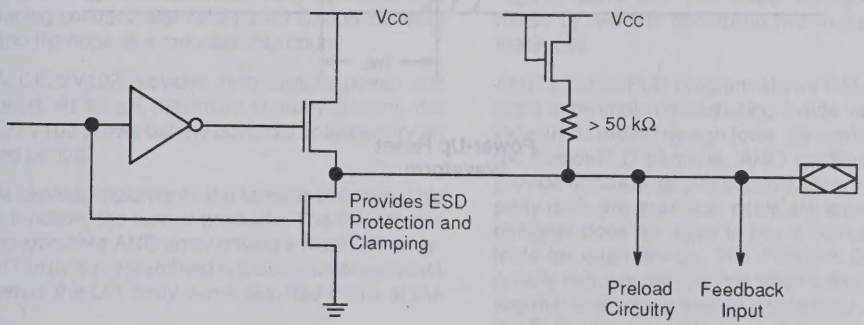
ROBUSTNESS FEATURES

The PALCE22V10H-10/5 has some unique features that make it extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSION



Typical Input



Typical Output

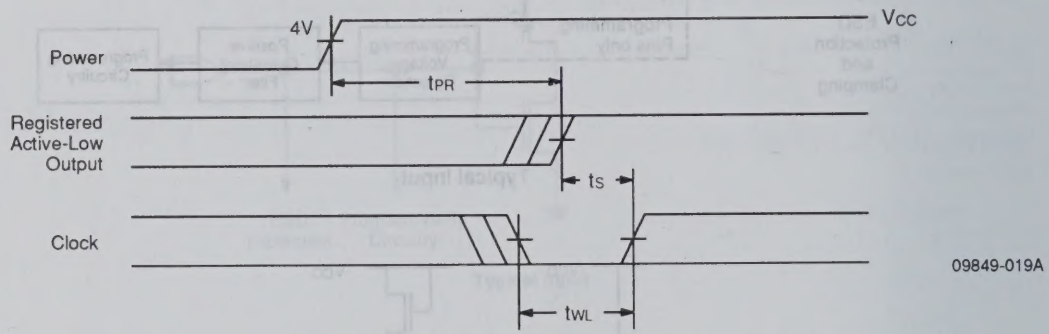
16407A-001B

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

PALCE22V10Z-25

Zero-Power 24-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Zero-power CMOS technology**
  - 15 µA standby current
  - 25 ns first-access propagation delay
- **Unused product term disable for reduced power consumption**
- **Industrial Operating Range**
  - T_C = −45°C to +85°C
  - V_{CC} = +4.5 V to +5.5 V
- **HC- and HCT-compatible inputs and outputs**
- **Electrically-erasable technology provides reconfigurable logic and full testability**
- **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- **Varied product term distribution allows up to 16 product terms per output for complex functions**
- **Global asynchronous reset and synchronous preset for initialization**
- **Power-up reset for initialization and register preload for testability**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **24-pin SKINNYDIP and 28-pin PLCC packages save space**

GENERAL DESCRIPTION

The PALCE22V10Z is an advanced PAL device built with zero-power, high-speed, electrically-erasable CMOS technology. It provides user-programmable logic for replacing conventional zero-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

The PALCE22V10Z provides zero standby power and high speed. At 15 µA maximum standby current, the PALCE22V10Z allows battery powered operation for an extended period.

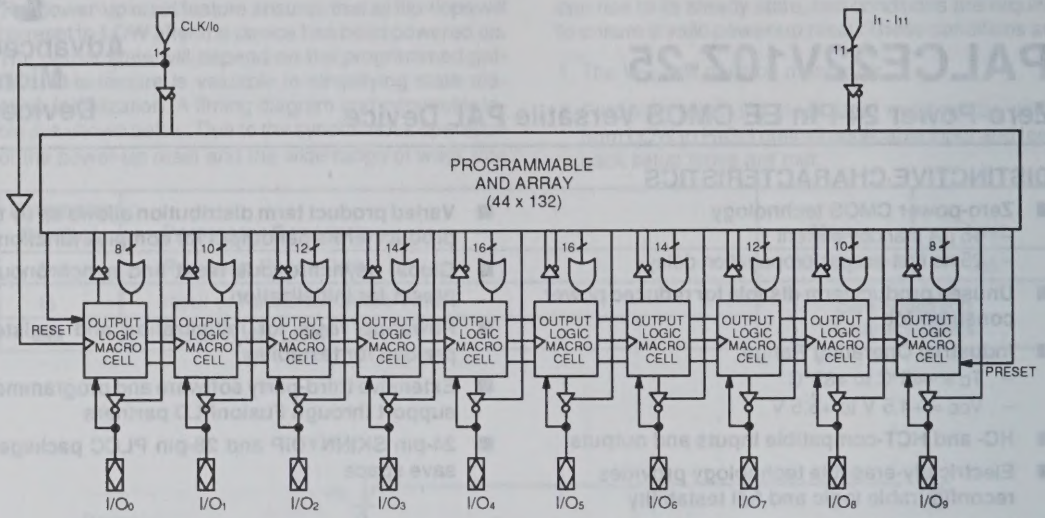
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 15700 Rev. A Amendment/0
Issue Date: January 1992

BLOCK DIAGRAM

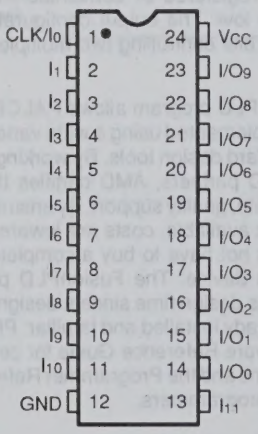


09849-001A

CONNECTION DIAGRAMS

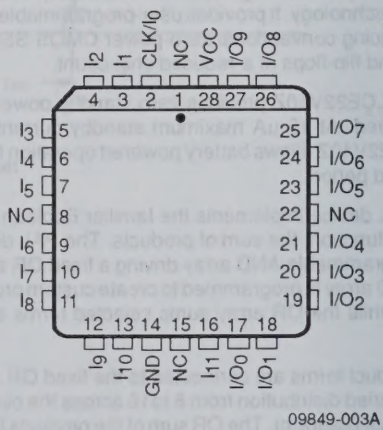
Top View

SKINNYDIP



09849-002A

PLCC



09849-003A

Note:

Pin 1 is marked for orientation.

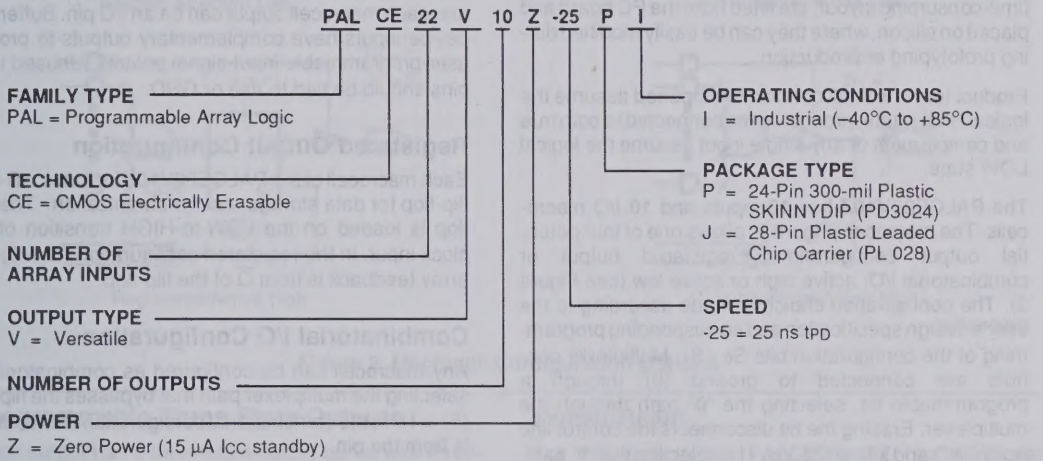
PIN DESCRIPTION

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
Vcc	=	Supply Voltage

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations	
PALCE22V10Z-25	PI, JI

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE22V10Z is the zero-power version of the PALCE22V10. It has all the architectural features of the PALCE22V10. In addition, the PALCE22V10Z has zero standby power and unused product term disable.

The PALCE22V10Z allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10Z has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 - S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

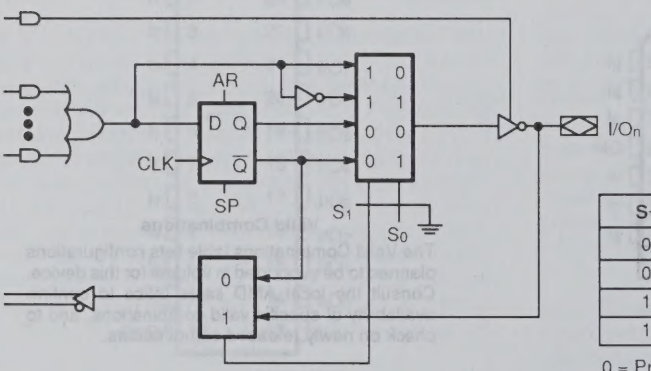
The PALCE22V10Z has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Registered Output Configuration

Each macrocell of the PALCE22V10Z includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

09849-004A

Figure 1. Output Logic Macrocell

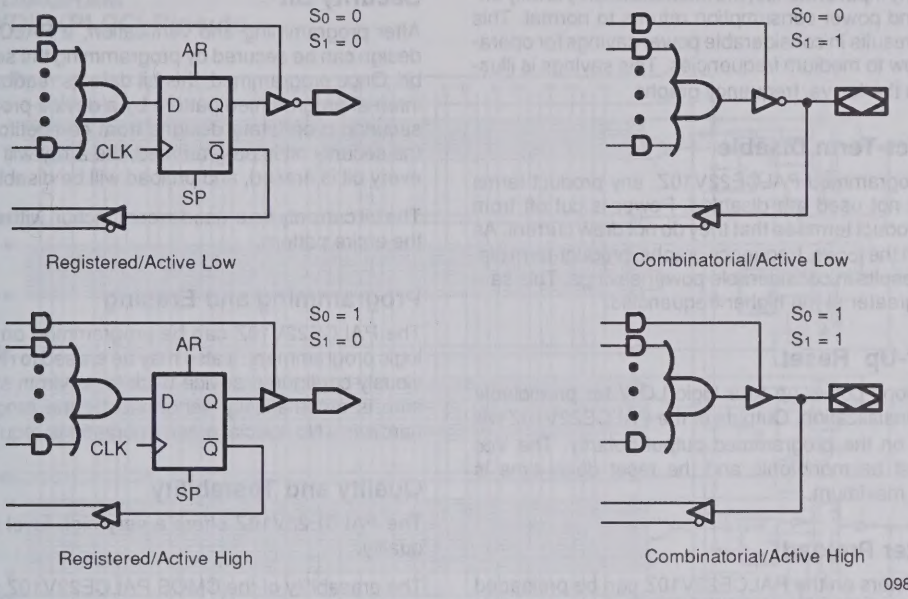


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10Z has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Zero-Standby Power Mode

The PALCE22V10Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE22V10Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero ($I_{CC} < 15\ \mu A$). The outputs will maintain the states held before the device went into the standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the Icc vs. frequency graphs.

Product-Term Disable

On a programmed PALCE22V10Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the Icc vs. frequency graphs, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10Z will depend on the programmed output polarity. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The registers on the PALCE22V10Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10Z design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

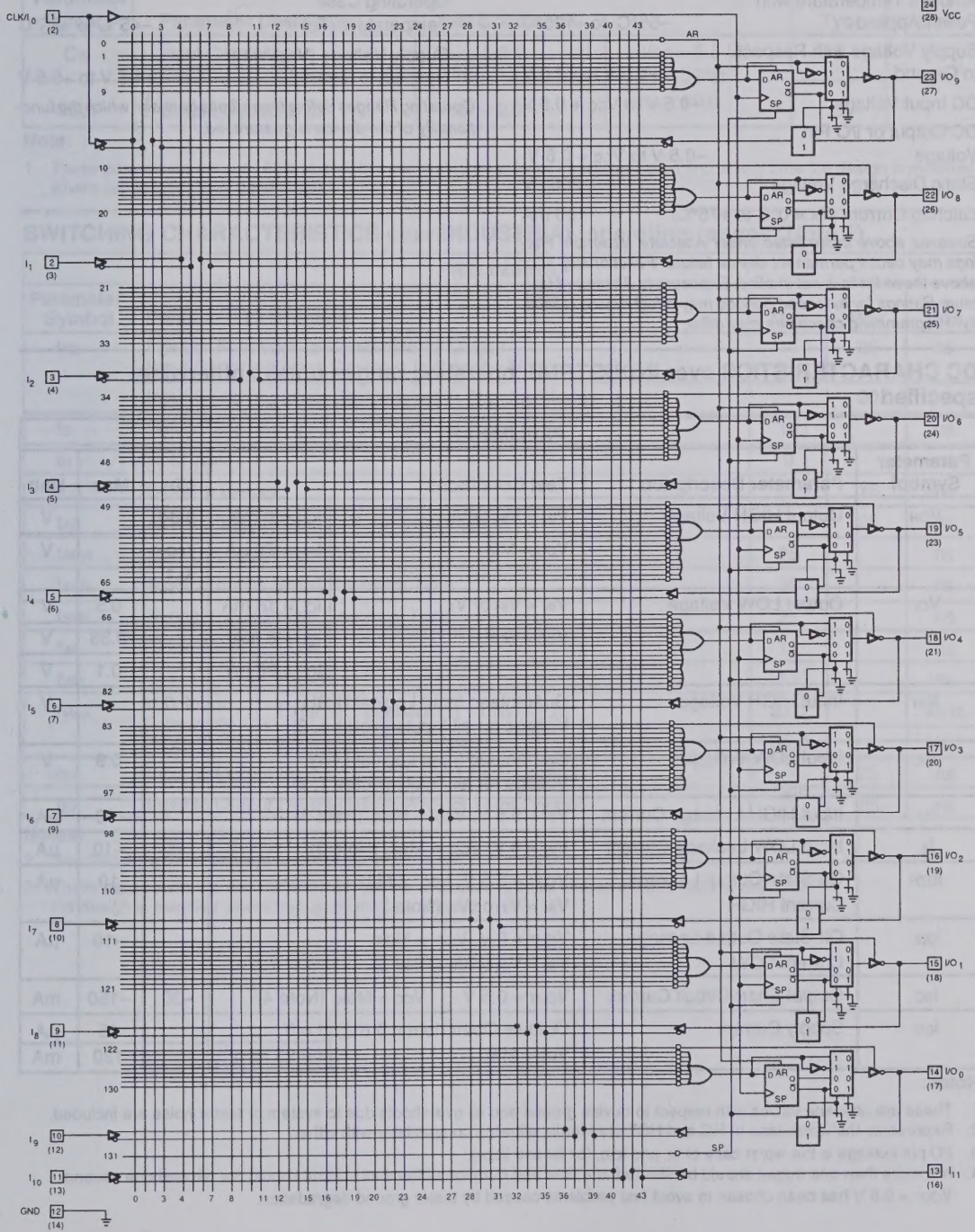
The PALCE22V10Z offers a very high level of built-in quality.

The erasability of the CMOS PALCE22V10Z allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The high-speed PALCE22V10Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts



09849-006A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case Temperature (T_C)	–45°C to +85°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 6 mA	3.84		V
		V_{CC} = Min.	I_{OH} = 20 µA	V_{CC}–0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
		V_{CC} = Min.	I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V V_{CC} = Max. (Note 4)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0		15	µA
		V_{CC} = Max.	f = 25 MHz		120	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Represents the worst case of HC and HCT standards, allowing compatibility with either.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

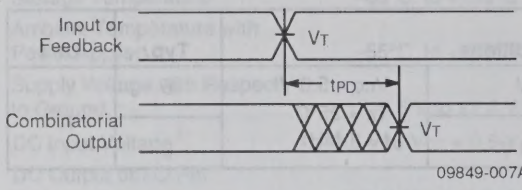
PRELIMINARY

Parameter Symbol	Parameter Description			Min.	Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output Input Switching when Device is in Standby Mode				25	ns
	Input Switching when Device is not in Standby Mode				20	ns
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		ns
t_{SPR}	Synchronous Preset Recovery Time			25		ns
t_{WL}	Clock Width	LOW		13		ns
t_{WH}		HIGH		13		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})		35.7		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

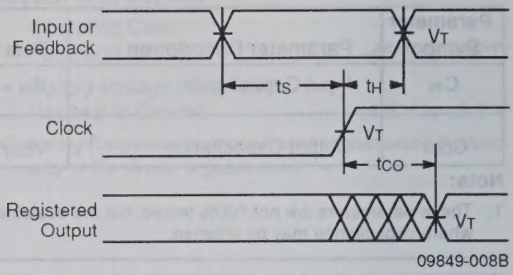
Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

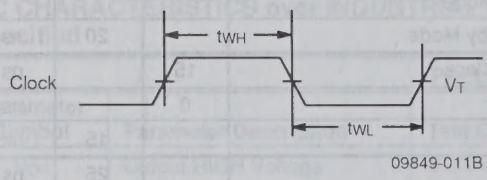
SWITCHING WAVEFORMS



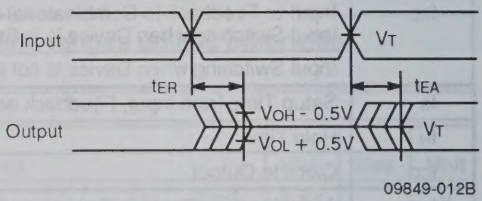
Combinatorial Output



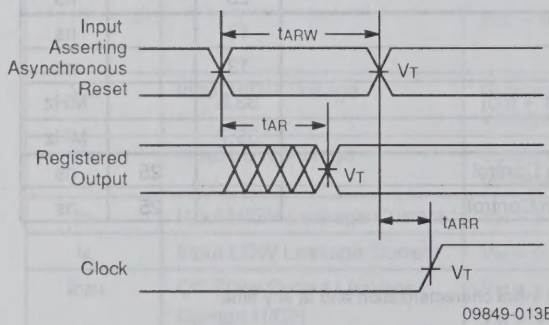
Registered Output



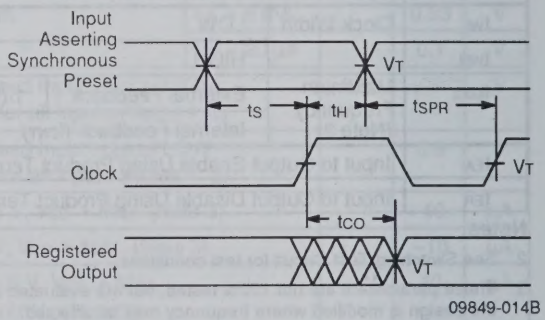
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

Notes:

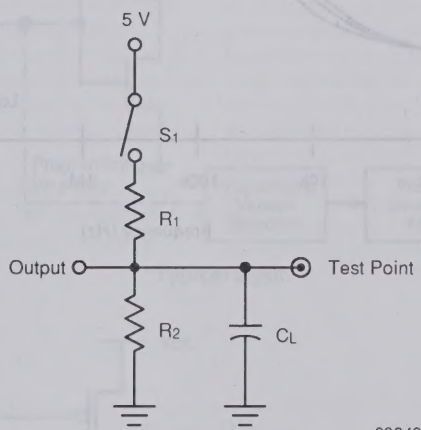
1. $V_T = V_{CC/2}$.
2. Input pulse amplitude 0 V to V_{CC}
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

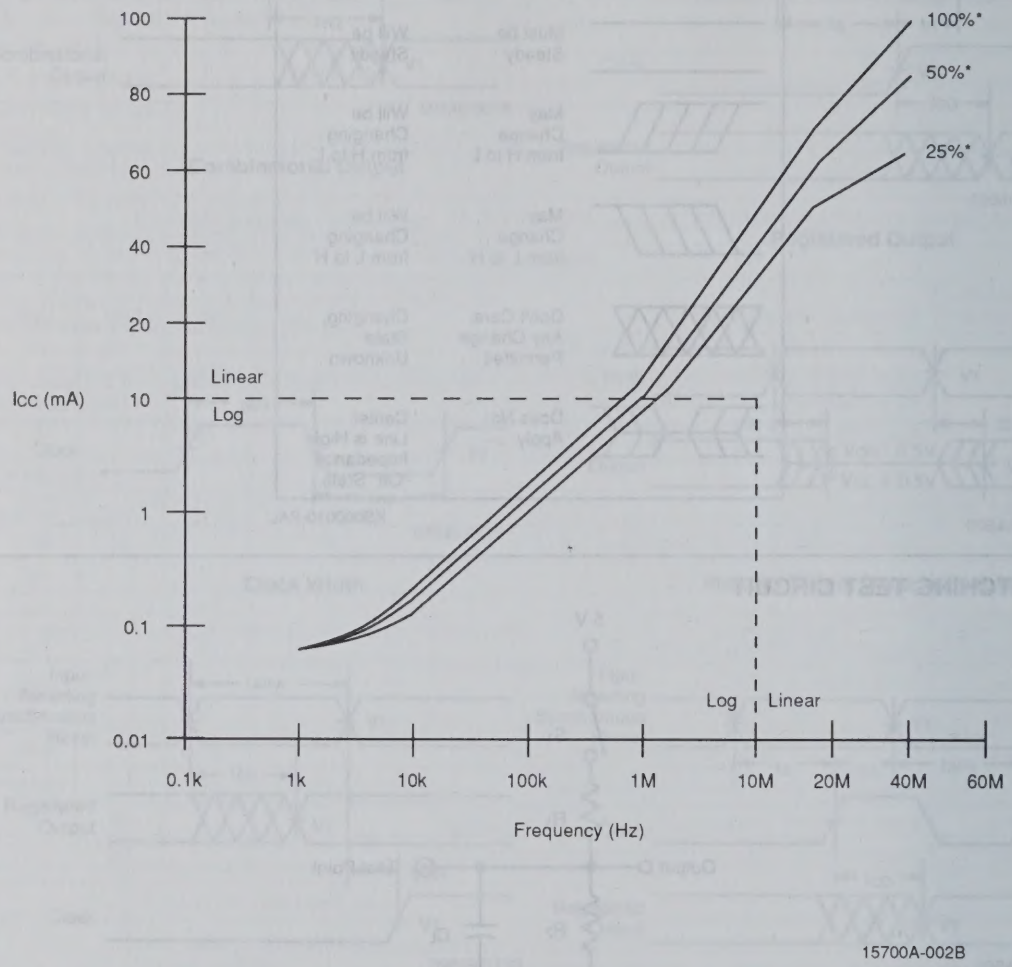
SWITCHING TEST CIRCUIT



09849-015A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	30 pF	820 Ω	820 Ω	$V_{CC}/2$
t_{EA}	Z → H: Open Z → L: Closed				$V_{CC}/2$
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5.0 V, T_A = 25°C



15700A-002B

*Percent of product terms used.

I_{CC} vs. Frequency

ENDURANCE CHARACTERISTICS

The PALCE22V10Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

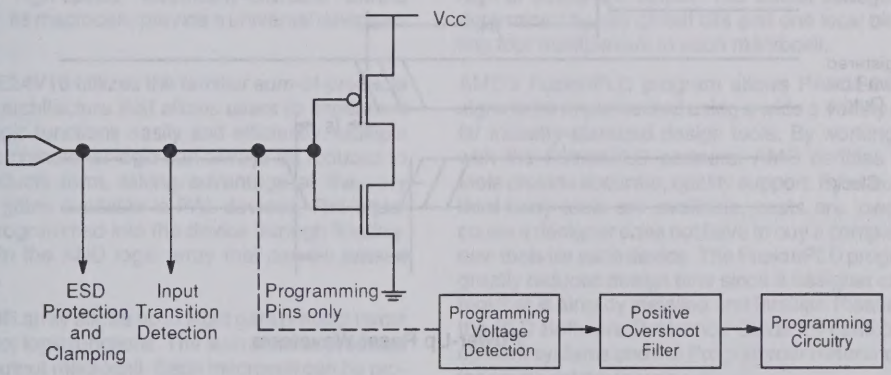
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	20	Years	Max. Operating Temperature
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

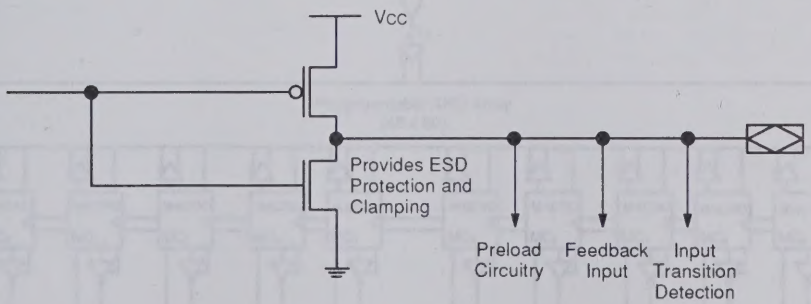
ROBUSTNESS FEATURES

The PALCE22V10Z-25 has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

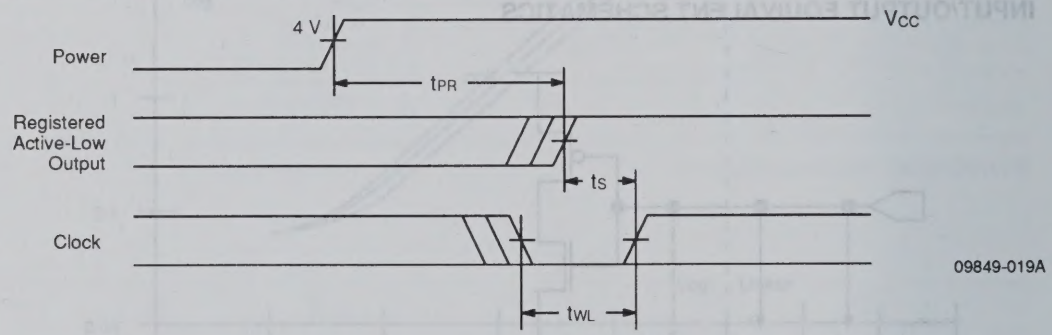
13061B-003A

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

PALCE24V10H-15/25

EE CMOS 28-Pin Universal Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High speed CMOS technology**
  - 15 ns propagation delay for "-15" version
  - 25 ns propagation delay for "-25" version
- **Outputs individually programmable as registered or combinatorial**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power-up**
- **Cost-effective 28-pin plastic SKINNYDIP and PLCC packages**
- **Extensive third-party support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**

GENERAL DESCRIPTION

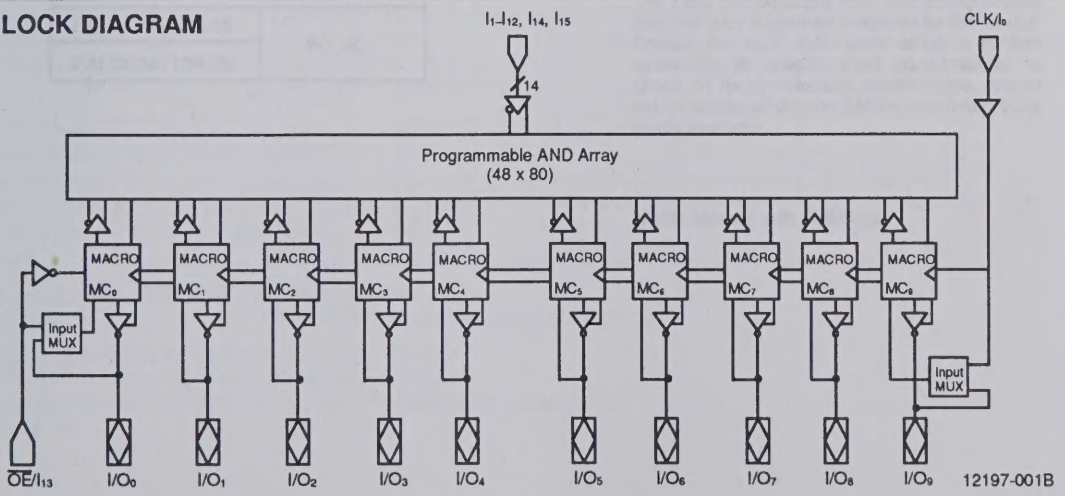
The PALCE24V10 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture.

The PALCE24V10 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE24V10 designs to be implemented using a wide a variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

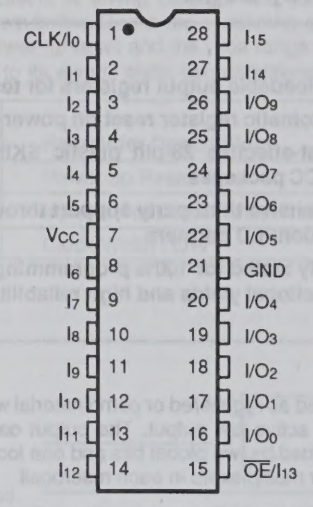
BLOCK DIAGRAM



Publication# 12222 Rev. D Amendment/0
Issue Date: January 1992

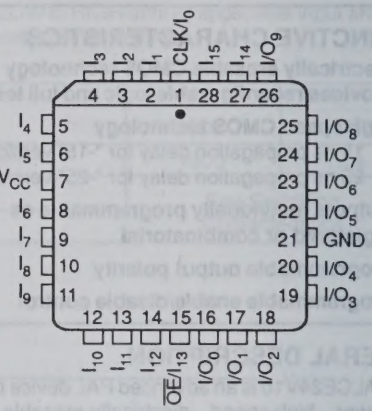
CONNECTION DIAGRAMS
Top View

SKINNYDIP



12222C-002B

PLCC



12222C-003A

Note:
Pin 1 is marked for orientation.

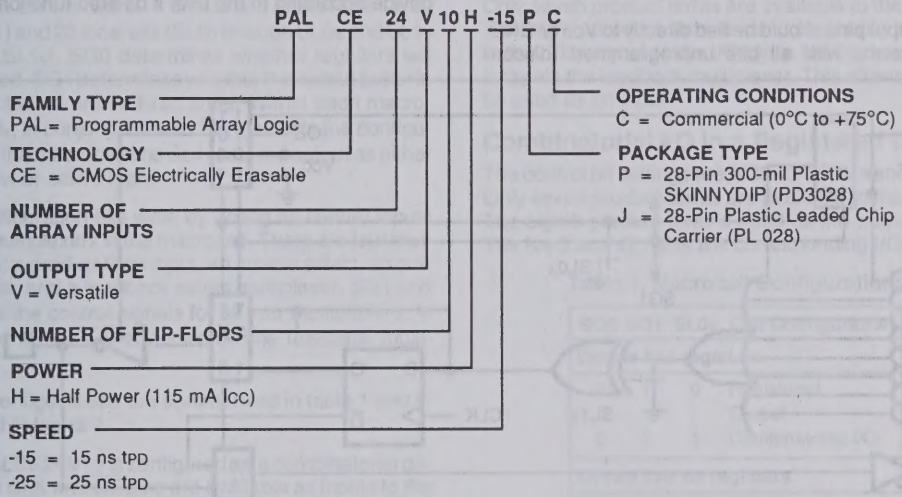
PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
$\overline{OE}$	=	Output Enable
Vcc	=	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE24V10H-15	PC, JC
PALCE24V10H-25	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

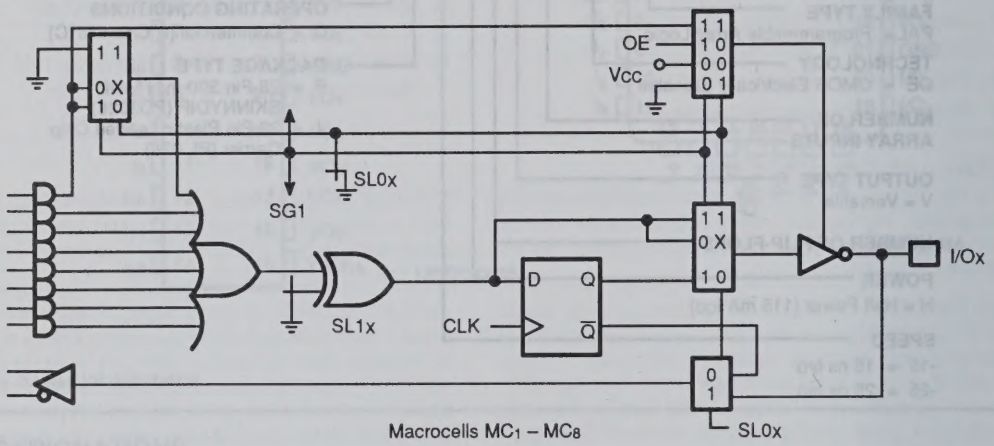
Note: Marked with AMD logo.

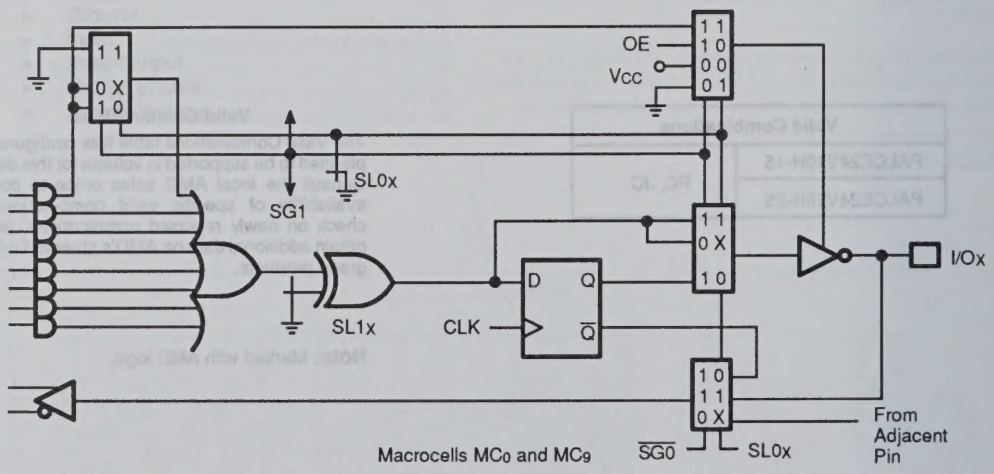
FUNCTIONAL DESCRIPTION

The PALCE24V10 is a universal PAL device. It has ten independently configurable macrocells ($MC_0..MC_9$). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 15 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$) for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE24V10 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.





12222C-004A

PALCE24V10 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled.

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 20 local bits ($SL0_0$ through $SL0_9$ and $SL1_0$ through $SL1_9$). SG0 determines whether registers will be allowed. SG1 determines whether the output buffer is user-controlled or in a fixed state. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell and $SL1_x$ sets the output as either active low or active high.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_9, $\overline{SG0}$ is added on the feedback multiplexer.

These configurations are summarized in table 1 and illustrated in figure 2.

If the PALCE24V10 is configured as a combinatorial device, the CLK and $\overline{OE}$ pins are available as inputs to the array. If the device is configured with registers, the CLK and $\overline{OE}$ pins cannot be used as data inputs.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. $SL1_x$ is an input to the exclusive-OR gate which is the D input to the flip-flop. $SL1_x$ is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE24V10 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 0, and $SL0_x$ = 0. All eight product terms are available to the OR gate. Because the macrocell is a dedicated output, the feedback is not used.

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. The feedback signal is the I/O pin.

Combinatorial I/O in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0,SG1=1 and $SL0_x$ =1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

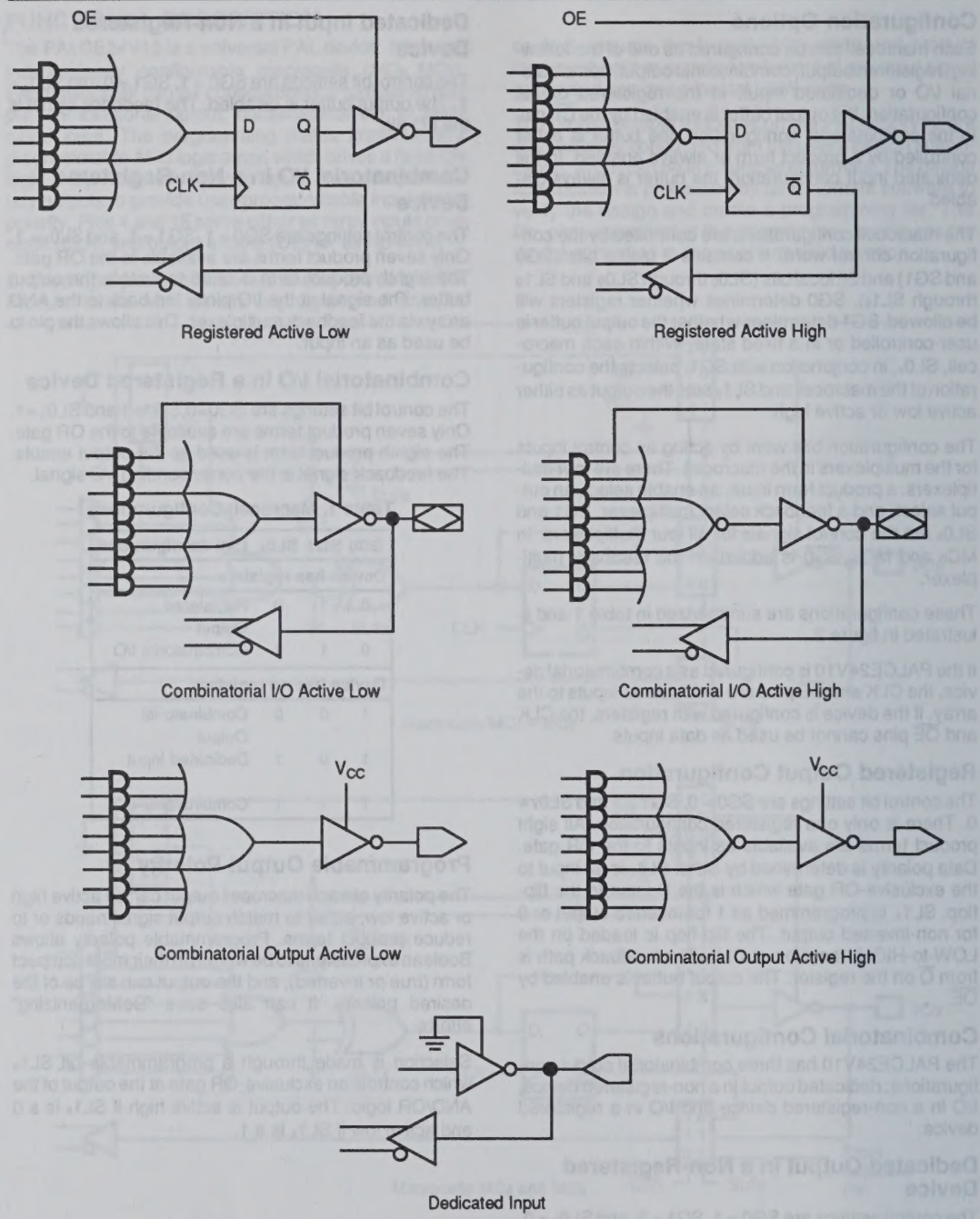
Table 1. Macrocell Configurations

SG0	SG1	$SL0_x$	Cell Configuration
Device has registers			
0	1	0	Registered Output
0	1	1	Combinatorial I/O
Device has no registers			
1	0	0	Combinatorial Output
1	0	1	Dedicated Input
1	1	1	Combinatorial I/O

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is made through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is a 0 and active low if $SL1_x$ is a 1.



12222C-005A

Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE24V10 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Register Preload

The register on the PALCE24V10 Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

A security bit is provided on the PALCE24V10 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE24V10. It consists of 64 bits of programmable memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE24V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

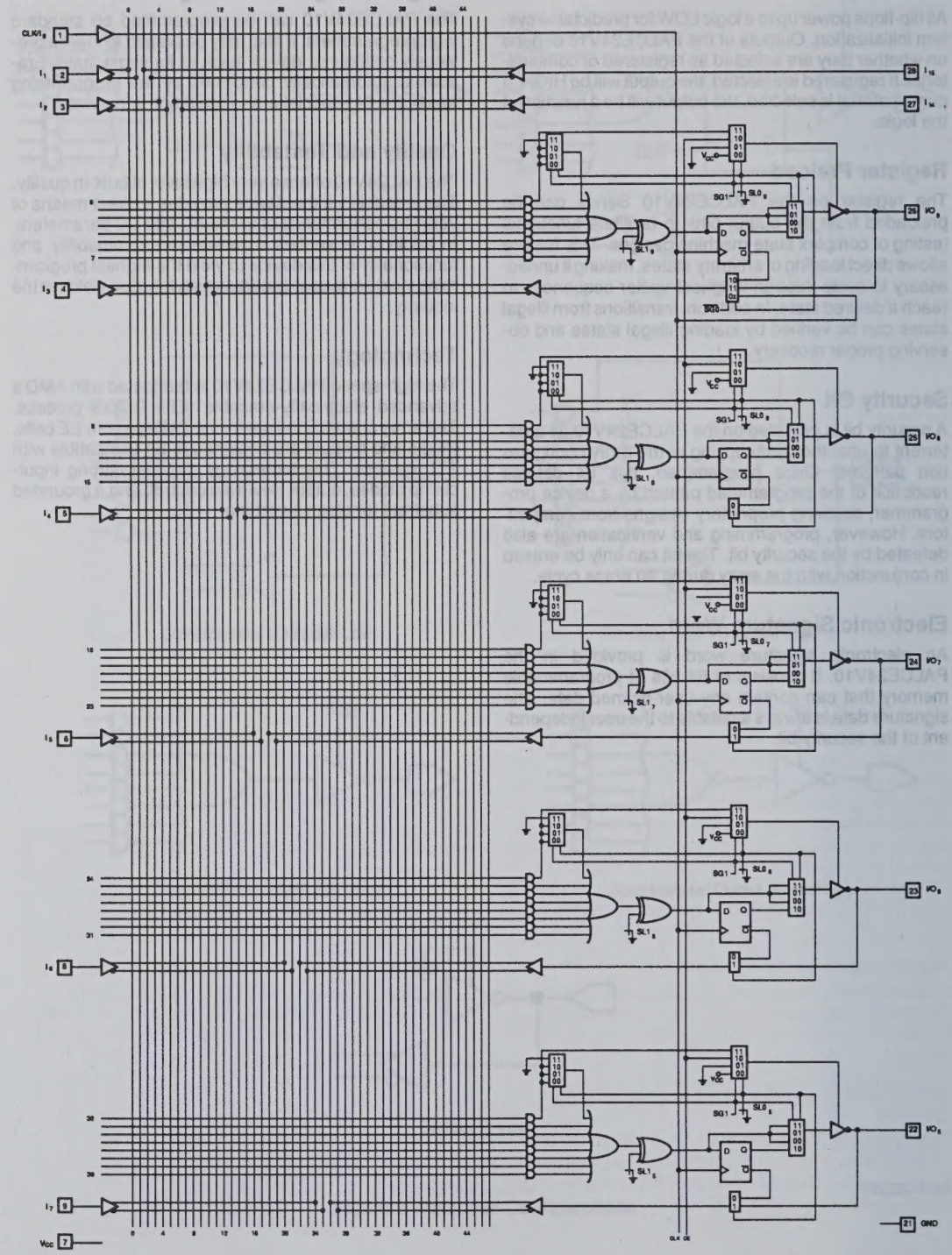
Quality and Testability

The PAL24V10 offers a very high level of built-in quality. The erasability if the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, is verifies complete programmability and functionality of this device to yield the highest programming yields and post-programming function yields in the industry.

Technology

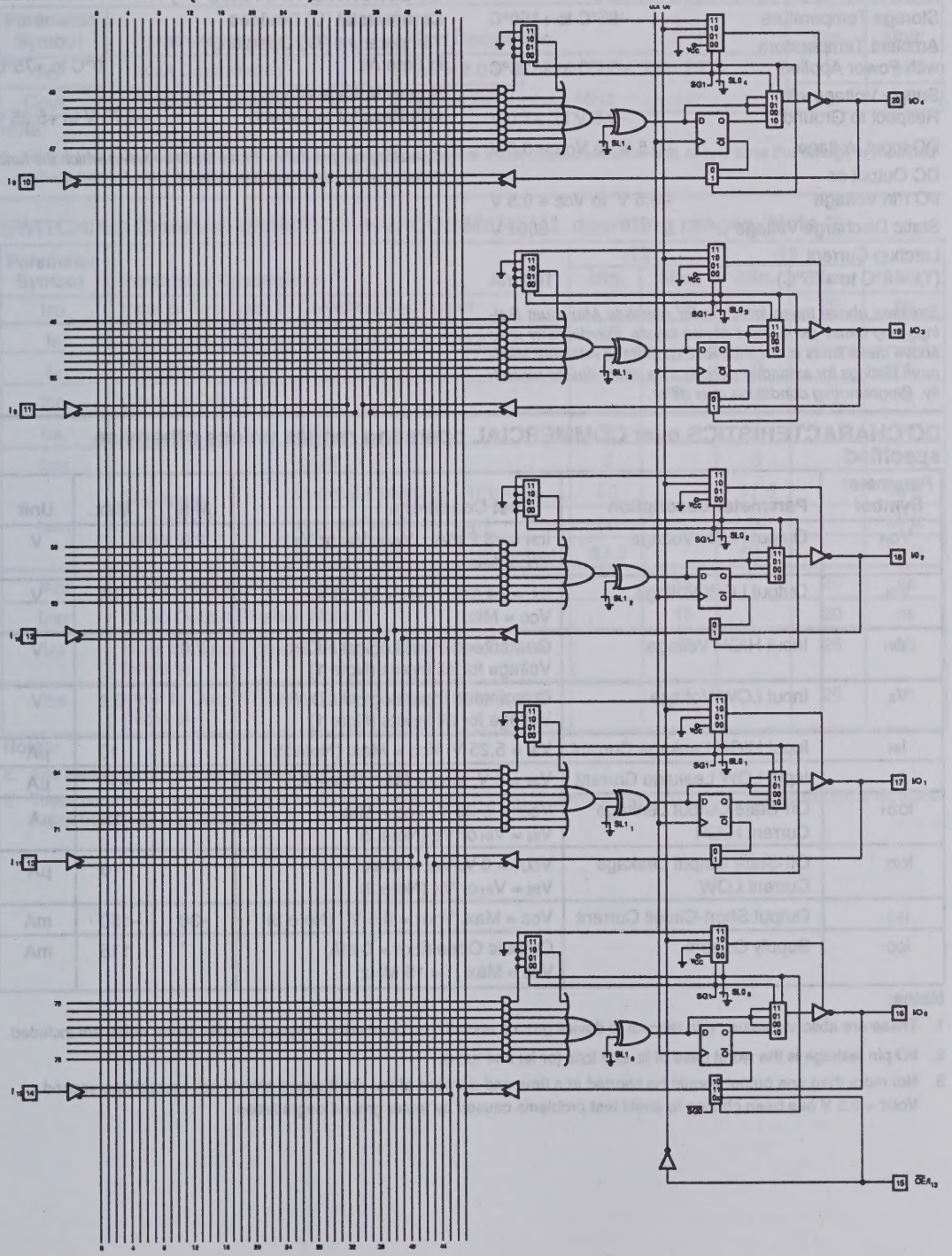
The high-speed PALCE24V10 is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM



12222C-006A

LOGIC DIAGRAM (Continued)



12222C-006A
concluded

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max. V_{OUT} = 0.5 V (Note 3)	–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 15 MHz		115	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

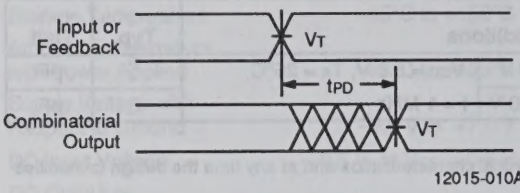
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			10		12		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{WL}	Clock Width	LOW		6		8		ns
t_{WH}		HIGH		6		8		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S+t_{CO})$	50		41.6		MHz
		Internal Feedback (f_{CNT})		66		50		MHz
		No Feedback	$1/(t_{WH}+t_{WL})$	83.3		62.5		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 3)				15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 3)				15		20	ns
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				15		25	ns

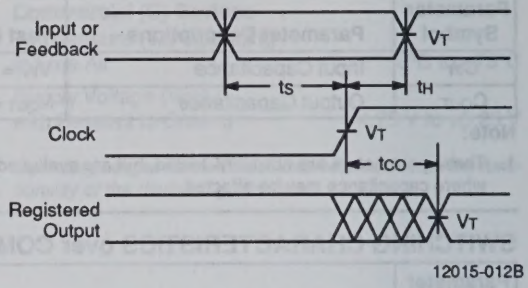
Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

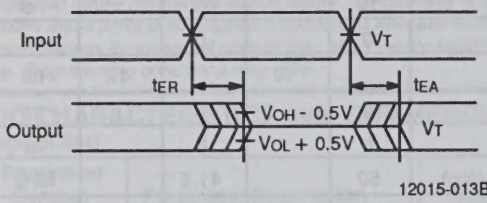
SWITCHING WAVEFORMS



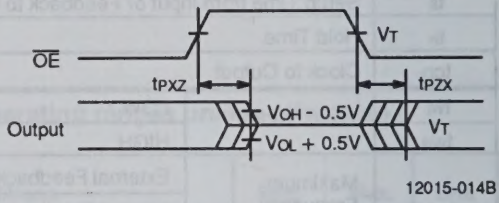
Combinatorial Output



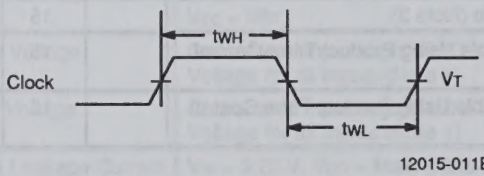
Registered Output



Input to Output Disable/Enable



$\overline{OE}$ to Output Disable/Enable



Clock Width

Notes:

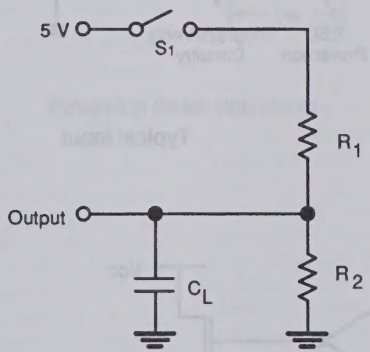
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12197-007A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF	200 Ω	390 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

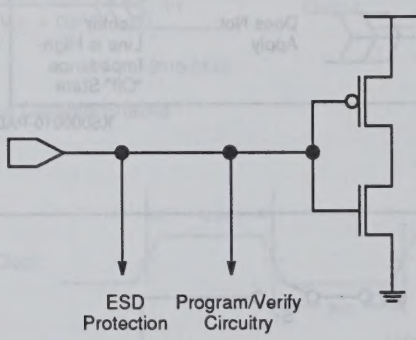
ENDURANCE CHARACTERISTICS

The PALCE24V10 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

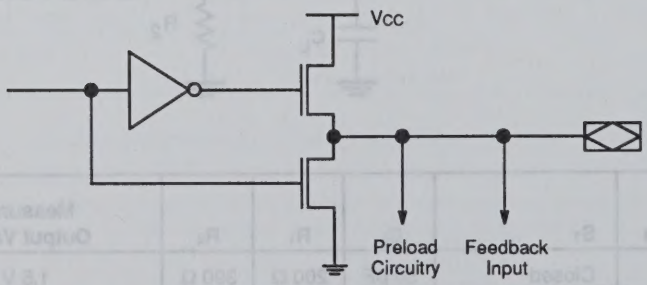
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

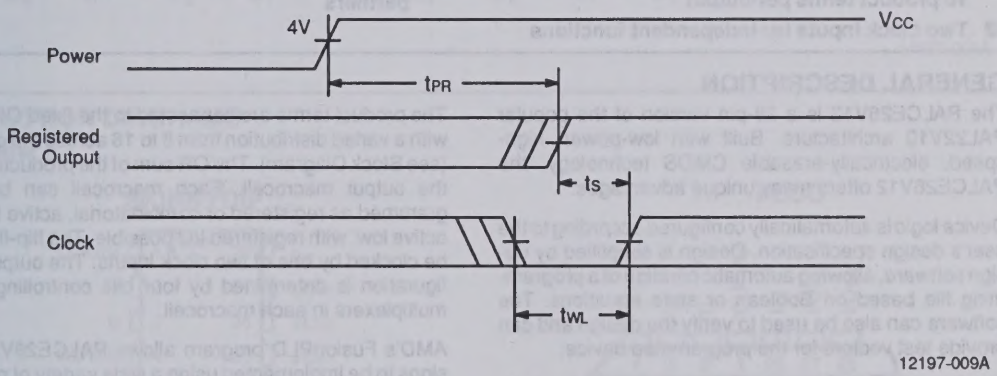
12197-013A

POWER-UP RESET

The PALCE24V10 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_{WL}	Clock Width LOW			



Power-Up Reset Waveform

PALCE26V12H-15/20

28-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 28-pin versatile PAL programmable logic device architecture
- Electrically erasable CMOS technology provides half power (only 105 mA) at high speed (15 ns propagation delay)
- 14 dedicated inputs and 12 input/output macrocells for architectural flexibility
- Macrocells can be registered or combinatorial, and active high or active low
- Varied product term distribution allows up to 16 product terms per output
- Two clock inputs for independent functions
- Global asynchronous reset and synchronous preset for initialization
- Register preload for testability and built-in register reset on power-up
- Space-efficient 28-pin SKINNYDIP and PLCC packages
- Center V_{CC} and GND pins to improve signal characteristics
- Extensive third-party software and programmer support through FusionPLD partners

GENERAL DESCRIPTION

The PALCE26V12 is a 28-pin version of the popular PAL22V10 architecture. Built with low-power, high-speed, electrically-erasable CMOS technology, the PALCE26V12 offers many unique advantages.

Device logic is automatically configured according to the user's design specification. Design is simplified by design software, allowing automatic creation of a programming file based on Boolean or state equations. The software can also be used to verify the design and can provide test vectors for the programmed device.

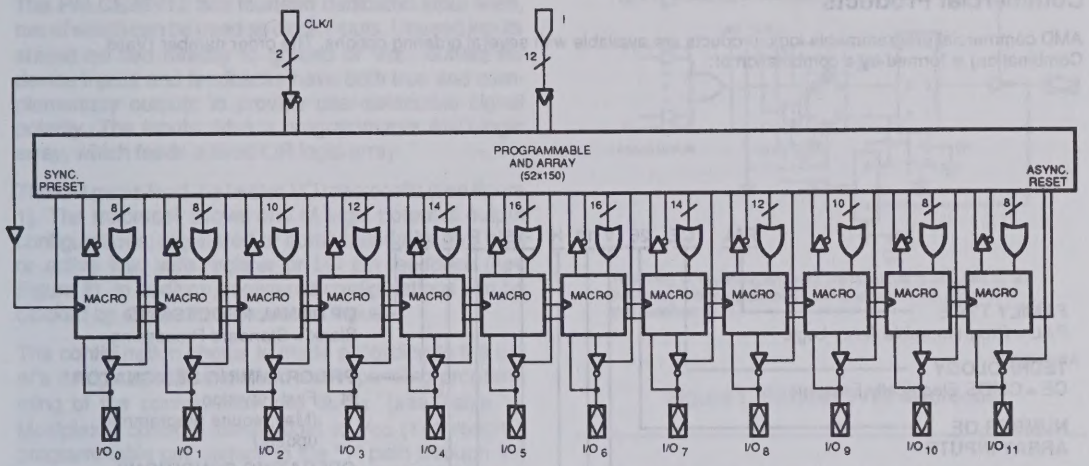
The PALCE26V12 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The functions are programmed into the device through electrically-erasable floating-gate cells in the AND logic array and the macrocells. In the unprogrammed state, all AND product terms float HIGH. If both true and complement of any input are connected, the term will be permanently LOW.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, active high or active low, with registered I/O possible. The flip-flop can be clocked by one of two clock inputs. The output configuration is determined by four bits controlling three multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE26V12 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

Publication# 16072 Rev. B Amendment/0
Issue Date: January 1992

BLOCK DIAGRAM



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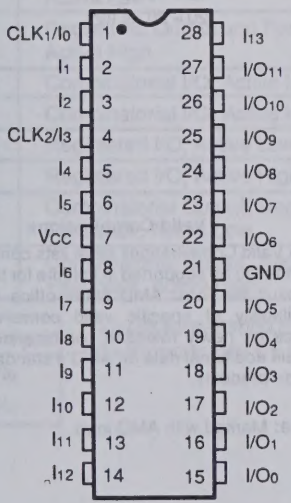
CONNECTION DIAGRAMS

Top View

SKINNYDIP



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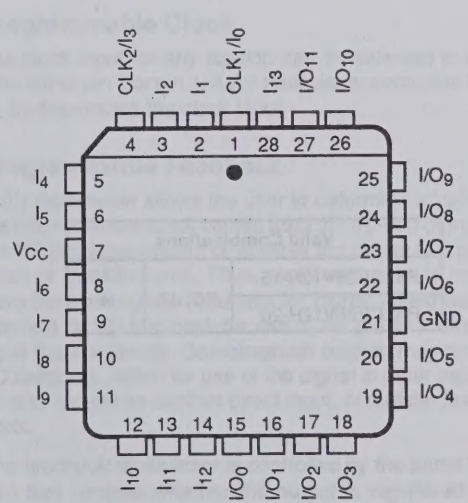
PLCC



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Note:
Pin 1 is marked for orientation.

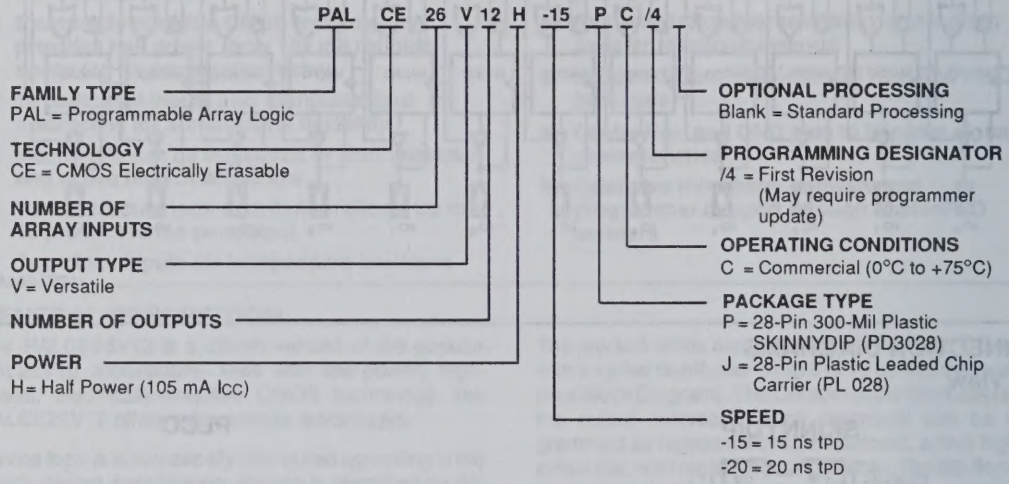
PIN DESCRIPTION

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD commercial programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE26V12H-15	PC, JC	/4
PALCE26V12H-20		

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

The PALCE26V12 has fourteen dedicated input lines, two of which can be used as clock inputs. Unused inputs should be tied directly to ground or V_{CC}. Buffers for device inputs and feedbacks have both true and complementary outputs to provide user-selectable signal polarity. The inputs drive a programmable AND logic array, which feeds a fixed OR logic array.

The OR gates feed the twelve I/O macrocells (see figure 1). The macrocell allows one of eight potential output configurations; registered or combinatorial, active high or active low, with register or I/O pin feedback (see Figure 2). In addition, registered configurations can be clocked by either of the two clock inputs.

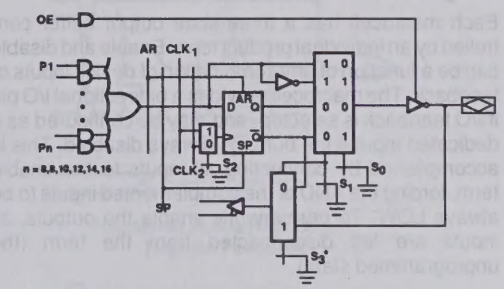
The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0-S_3 (see Table 1). Multiplexer controls initially float to V_{CC} (1) through a programmable cell, selecting the "1" path through the multiplexer. Programming the cell connects the control line to GND (0), selecting the "0" path.

Table 1. Macrocell Configuration Table

S_3	S_1	S_0	Output Configuration
1	0	0	Registered Output and Feedback, Active Low
1	0	1	Registered Output and Feedback, Active High
1	1	0	Combinatorial I/O, Active Low
1	1	1	Combinatorial I/O, Active High
0	0	0	Registered I/O, Active Low
0	0	1	Registered I/O, Active High
0	1	0	Combinatorial Output, Registered Feedback, Active Low
0	1	1	Combinatorial Output, Registered Feedback, Active High

S_2	Clock Input
1	CLK_1/I_0
0	CLK_2/I_3

1 = Unprogrammed EE bit
0 = Programmed EE bit



*When S_3 = 1 (unprogrammed) the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

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Figure 1. PALCE26V12 Macrocell

Registered or Combinatorial

Each macrocell of the PALCE26V12 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH edge of the selected clock input. Any macrocell can be configured as combinatorial by selecting a multiplexer path that bypasses the flip-flop. Bypass is controlled by bit S_1.

Programmable Clock

The clock input for any flip-flop can be selected to be from either pin 1 or pin 4. A 2:1 multiplexer controlled by bit S_2 determines the clock input.

Programmable Feedback

A 2:1 multiplexer allows the user to determine whether the macrocell feedback comes from the flip-flop or from the I/O pin, independent of whether the output is registered or combinatorial. Thus, registered outputs may have internal register feedback for higher speed (f_{MAX} internal), or I/O feedback for use of the pin as a direct input (f_{MAX} external). Combinatorial outputs may have I/O feedback, either for use of the signal in other equations or for use as another direct input, or register feedback.

The feedback multiplexer is controlled by the same bit (S_1) that controls whether the output is registered or combinatorial, as on the 22V10, with an additional control bit (S_3) that allows the alternative feedback path to be selected. When S_3 = 1, S_1 selects register feedback for registered outputs (S_1 = 0) and I/O feedback for combinatorial outputs (S_1 = 1). When S_3 = 0, the opposite is selected: I/O feedback for registered outputs and register feedback for combinatorial outputs.

Programmable Enable and I/O

Each macrocell has a three-state output buffer controlled by an individual product term. Enable and disable can be a function of any combination of device inputs or feedback. The macrocell provides a bidirectional I/O pin if I/O feedback is selected, and may be configured as a dedicated input if the buffer is always disabled. This is accomplished by connecting all inputs to the enable term, forcing the AND of the complemented inputs to be always LOW. To permanently enable the outputs, all inputs are left disconnected from the term (the unprogrammed state).

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high.

Preset/Reset

For initialization, the PALCE26V12 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH or the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE26V12 will be HIGH or LOW depending on whether the output is active low or active high, respectively. The V_{CC} rise must be monotonic, and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE26V12 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE26V12 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. Programming the security bit disables preload, and the array will read as if every bit is disconnected. The security bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

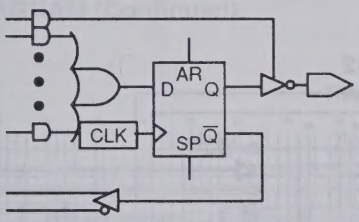
The PALCE26V12 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

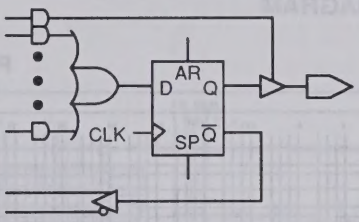
The PALCE26V12 offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

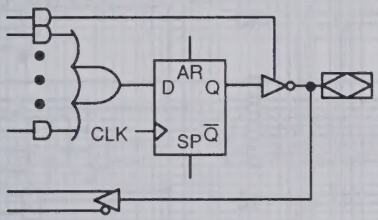
The high-speed PALCE26V12 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.



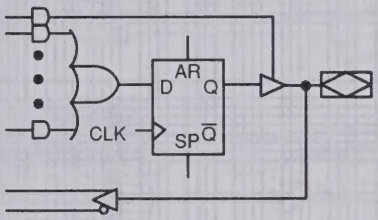
Registered Active-Low Output,
Register Feedback



Registered Active-High Output,
Register Feedback

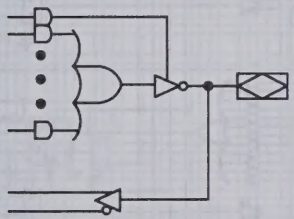


Registered Active-Low I/O

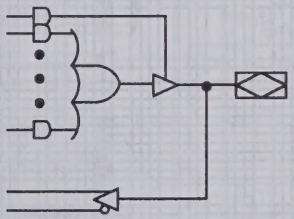


Registered Active-High I/O

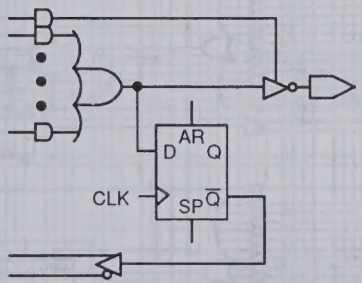
Registered Outputs



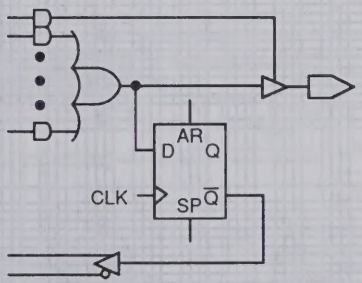
Combinatorial Active-Low I/O



Combinatorial Active-High I/O



Combinatorial Active-Low Output,
Register Feedback



Combinatorial Active-High Output,
Register Feedback

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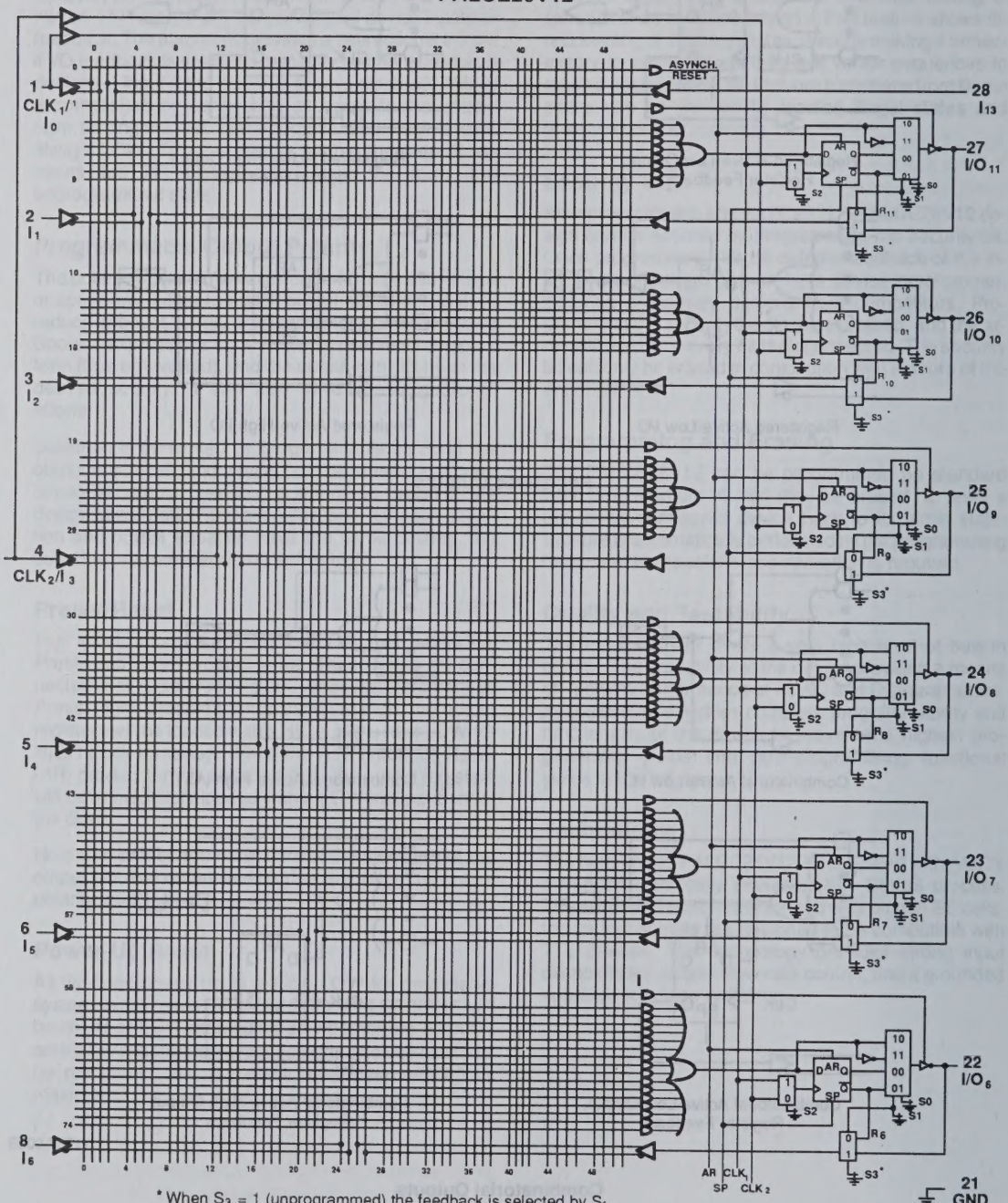
Combinatorial Outputs

Figure 2. PALCE26V12 Macrocell Configuration Options

LOGIC DIAGRAM

PALCE26V12



*When S_3 = 1 (unprogrammed) the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

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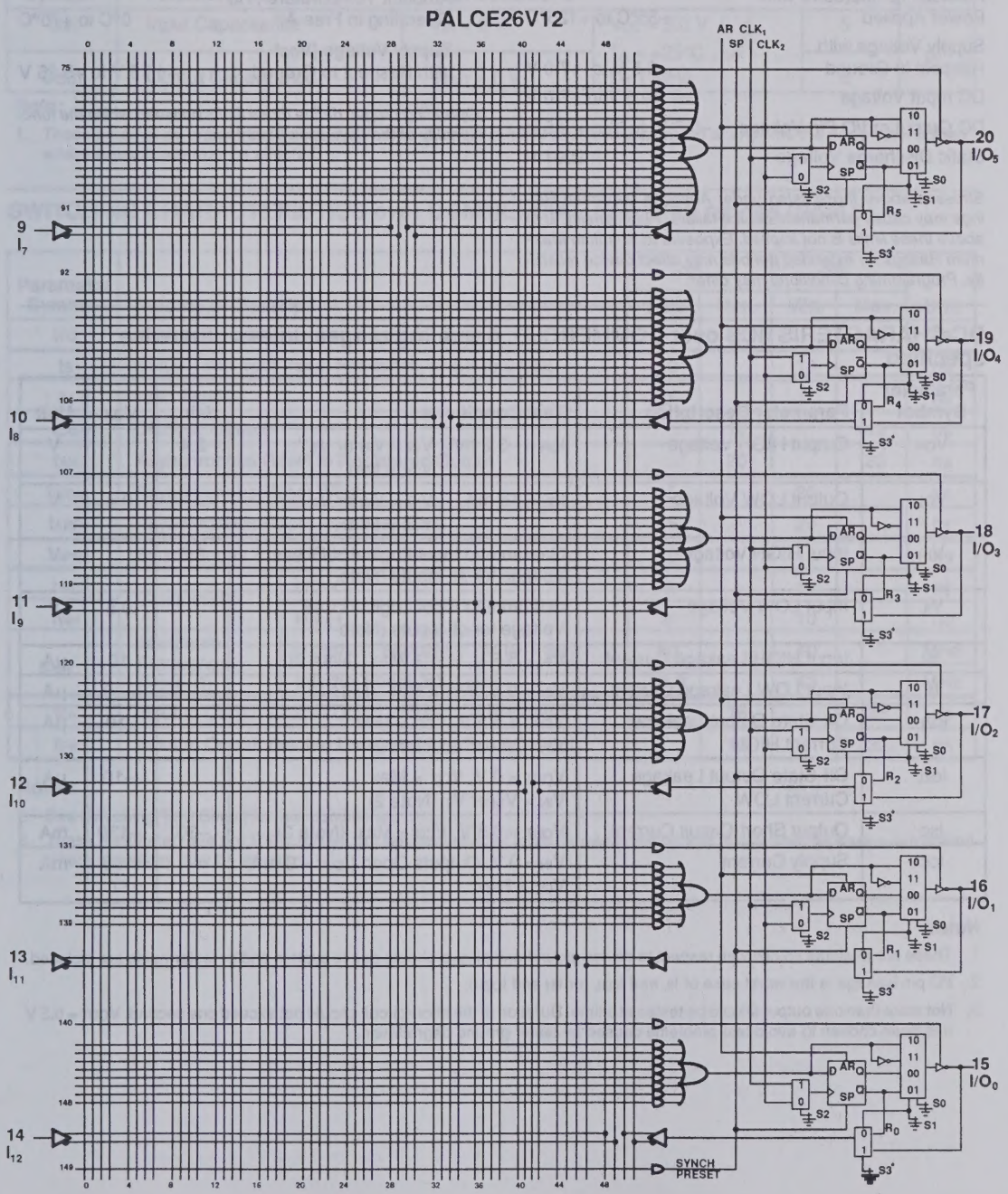
LOGIC DIAGRAM (Continued)



*When S_3 = 1 (unprogrammed) the feedback is selected by S_1. When S_3 = 0 (programmed), the feedback is the opposite of that selected by S_1.

11757-006A
(Concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.6 V to +7.0 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		105	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

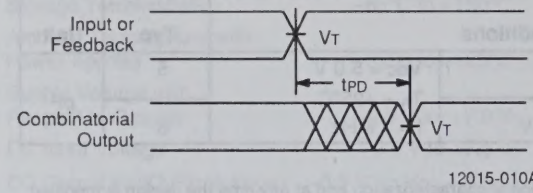
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		20	ns
t_S	Setup Time from Input, Feedback, or SP to Clock			10		13		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		12	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time			15		20		ns
t_{SPR}	Synchronous Preset Recovery Time			10		13		ns
t_{WL}	Clock Width	LOW		8		10		ns
t_{WH}		HIGH		8		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	1/(ts + tco)	50		40		MHz
		Internal Feedback (f_{CNT})		58.8		43		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		20	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		20	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



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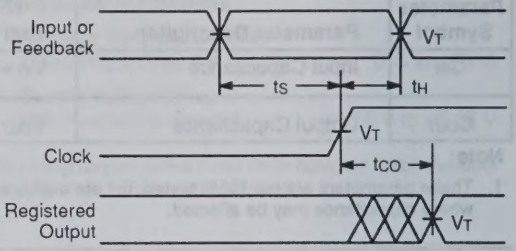
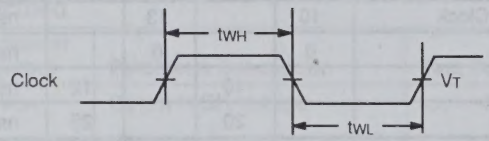
Combinatorial Output



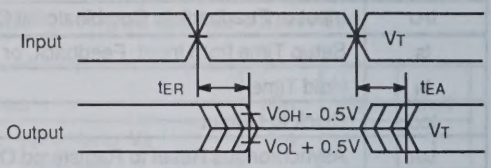
12015-012B

Registered Output



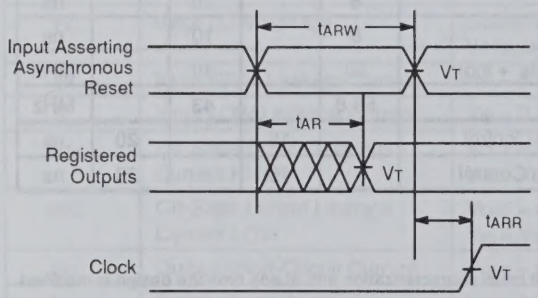
12015-011B

Clock Width



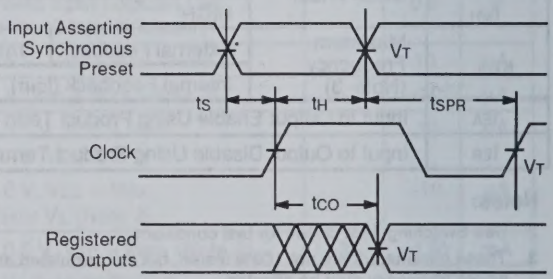
12015-013B

Input to Output Disable/Enable



11757-009B

Asynchronous Reset



11757-010B

Synchronous Preset

Notes:

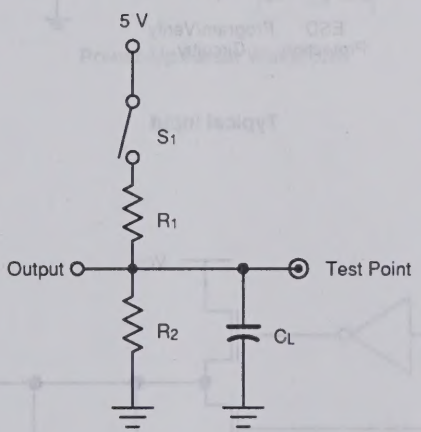
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12350-019A

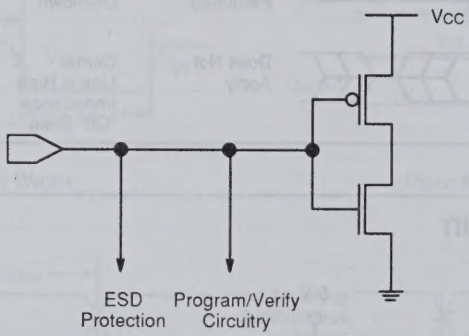
Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

ENDURANCE CHARACTERISTICS

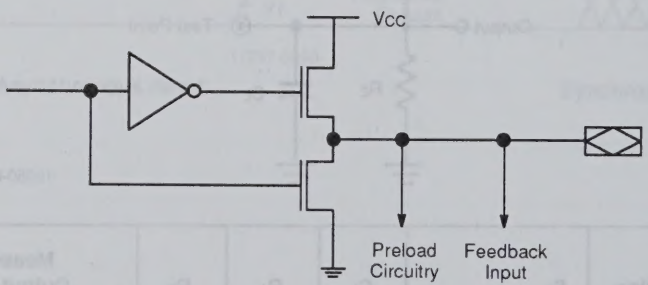
The PALCE26V12 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

Symbol	Parameter	Min.	Unit	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

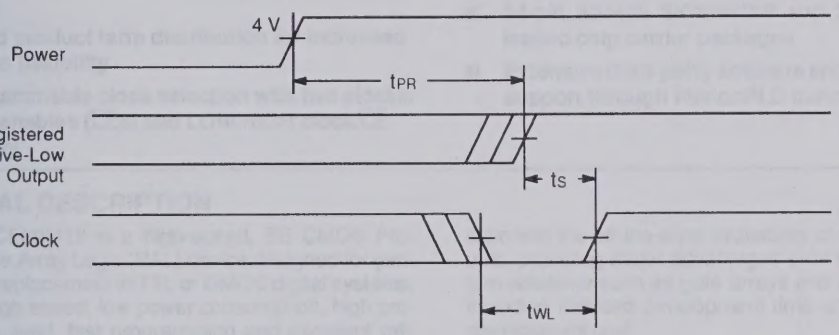
12197-013A

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

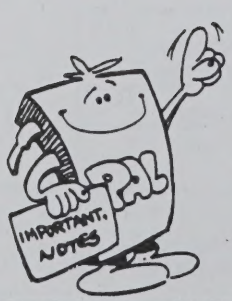
1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform


IMPORTANT
NOTES

PALCE29M16H-25

24-Pin EE CMOS Programmable Array Logic

Advanced Micro Devices

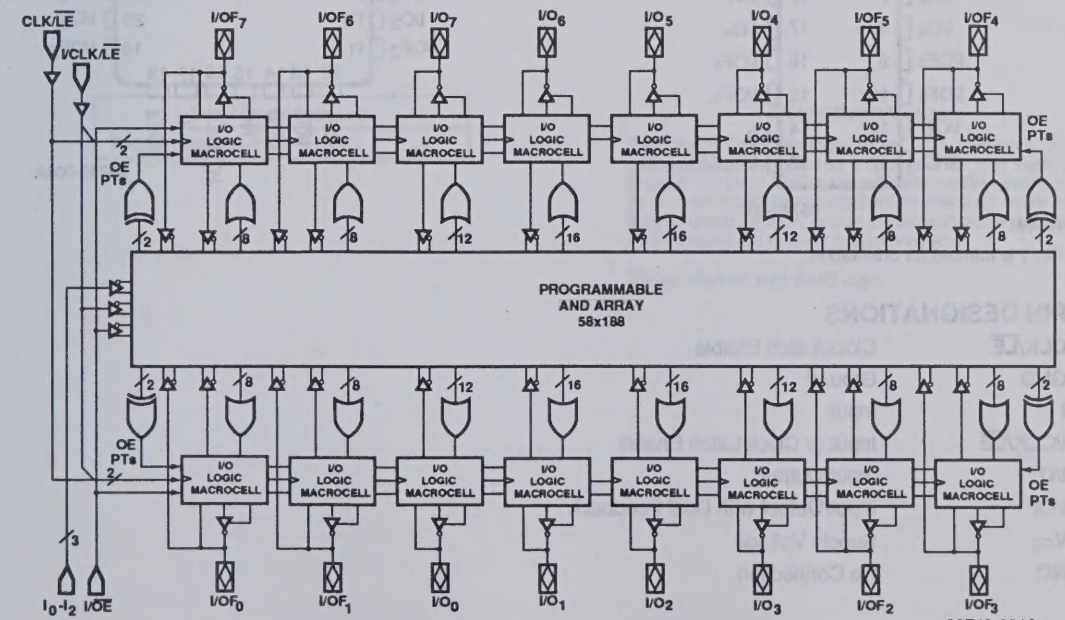
DISTINCTIVE CHARACTERISTICS

- High-performance semicustom logic replacement; Electrically Erasable (EE) technology allows reprogrammability
- 16 bidirectional user-programmable I/O logic macrocells for Combinatorial/Registered/ Latched operation
- Output Enable controlled by a pin or product terms
- Varied product term distribution for increased design flexibility
- Programmable clock selection with two clocks/ latch enables ($\overline{LE}$s) and LOW/HIGH clock/$\overline{LE}$ polarity
- Register/Latch Preload permits full logic verification
- High speed (t_{PD} = 25 ns, f_{MAX} = 33 MHz and f_{MAX} internal = 50 MHz)
- Full-function AC and DC testing at the factory for high programming and functional yields and high reliability
- 24-pin 300-mil SKINNYDIP and 28-pin plastic leaded chip carrier packages
- Extensive third-party software and programmer support through FusionPLD partners

GENERAL DESCRIPTION

The PALCE29M16 is a high-speed, EE CMOS Programmable Array Logic (PAL) device designed for general logic replacement in TTL or CMOS digital systems. It offers high speed, low power consumption, high programming yield, fast programming and excellent reliability. PAL devices combine the flexibility of custom logic with the off-the-shelf availability of standard products, providing major advantages over other semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.

BLOCK DIAGRAM



08740-001A

Publication# 08740 Rev. F Amendment/0
Issue Date: January 1992

GENERAL DESCRIPTION (Continued)

The PALCE29M16 uses the familiar sum-of-products (AND-OR) structure, allowing users to customize logic functions by programming the device for specific applications. It provides up to 29 array inputs and 16 outputs. It incorporates AMD's unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as combinatorial, registered, or latched with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the PALCE29M16 by providing a varied number of logic product terms per output. Eight outputs have 8 product terms each, four outputs have 12 product terms each, and the other four outputs have 16 product terms each. This varied product-term distribution allows complex functions to be implemented in a single PAL device. Each output can be dynamically controlled by a common Output Enable pin or Output Enable product terms per bank of four outputs. Each output can also be permanently enabled or disabled.

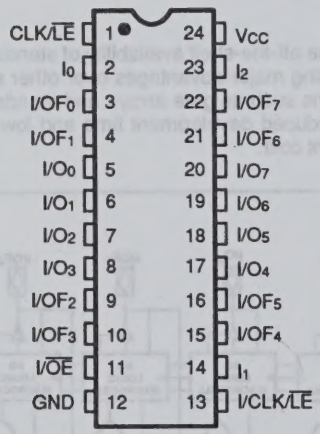
System operation has been enhanced by the addition of common asynchronous-Preset and Reset product terms and a power-up Reset feature. The PALCE29M16 also incorporates Preload and Observability functions which permit full logic verification of the design.

The PALCE29M16 is offered in the space-saving 300-mil SKINNYDIP package as well as the plastic leaded chip carrier package.

CONNECTION DIAGRAMS

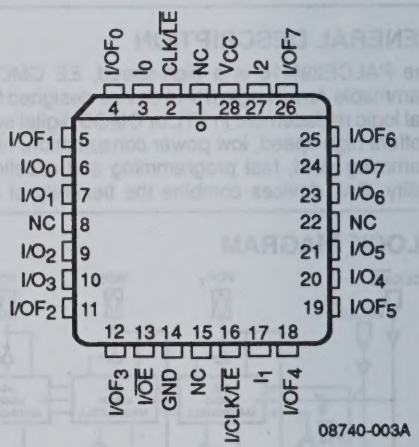
Top View

SKINNYDIP



08740-002A

PLCC



08740-003A

Note:
Pin 1 is marked for orientation.

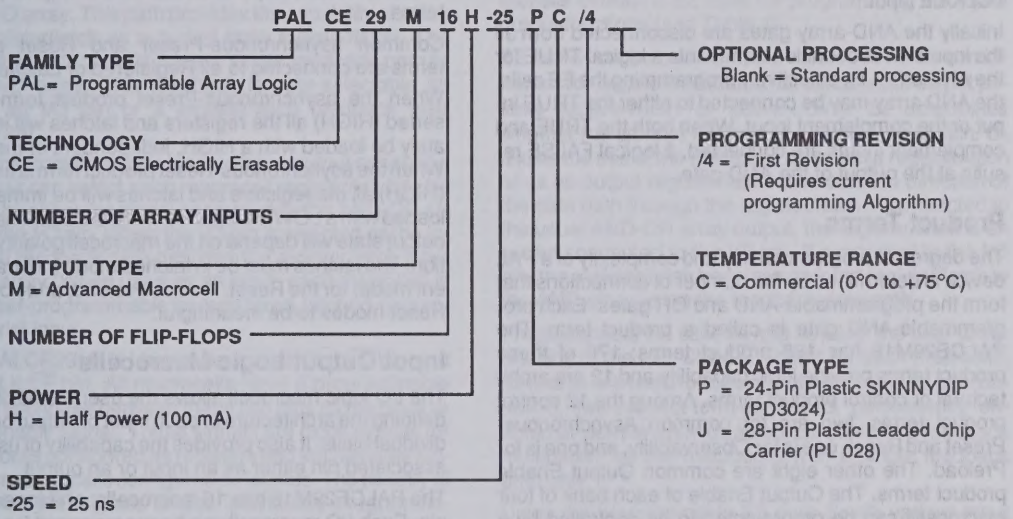
PIN DESIGNATIONS

CLK/$\overline{LE}$	Clock/Latch Enable
GND	Ground
I	Input
I/CLK/$\overline{LE}$	Input or Clock/Latch Enable
I/O	Input/Output
I/OF	Input/Output with Dual Feedback
Vcc	Supply Voltage
NC	No Connection

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE29M16H-25	PC, JC	/4

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

Inputs

The PALCE29M16 has 29 inputs to drive each product term (up to 58 inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram in Figure 1. Of these 29 inputs, 3 are dedicated inputs, 16 are from 8 I/O logic macrocells with two feedbacks, 8 are from other I/O logic macrocells with single feedback, one is the I/$\overline{OE}$ input and one is the I/CLK/$\overline{LE}$ input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE for the AND array. By selectively programming the EE cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The PALCE29M16 has 188 product terms; 176 of these product terms provide logic capability and 12 are architectural or control product terms. Among the 12 control product terms, two are for common Asynchronous-Preset and Reset, one is for Observability, and one is for Preload. The other eight are common Output Enable product terms. The Output Enable of each bank of four macrocells can be programmed to be controlled by a common Output Enable pin or two AND/XOR product terms. It may be also permanently enabled or permanently disabled.

Each product term on the PALCE29M16 consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a varied distribution across the device ranging from 8 to 16 wide, with an average of 11 logic product terms per output. An increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

Common asynchronous-Preset and Reset product terms are connected to all Registered or Latched I/Os.

When the asynchronous-Preset product term is asserted (HIGH) all the registers and latches will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-Reset product term is asserted (HIGH) all the registers and latches will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the Reset, Preset, Preload, and power-up Reset modes to be meaningful.

Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The PALCE29M16 has 16 macrocells, one for each I/O pin. Each I/O macrocell can be programmed for combinatorial, registered or latched operation (see Figure 2). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers and Latches are used in synchronous logic applications.

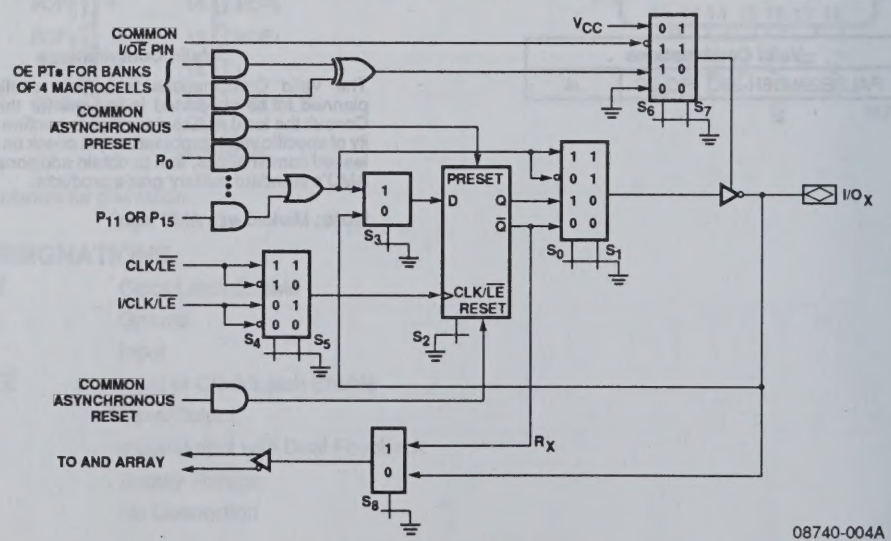


Figure 2a. PALCE29M16 Macrocell (Single Feedback)

The output polarity for each macrocell in each of the three modes of operation is user-selectable, allowing complete flexibility of the macrocell configuration.

Eight of the macrocells (I/OF_0–I/OF_7) have two independent feedback paths to the AND array (see Figure 2b). The first is a dedicated I/O pin feedback to the AND array for combinatorial input. The second path consists of a direct register/latch feedback to the array. If the pin is used as a dedicated input using the first feedback path, the register/latch feedback path is still available to the AND array. This path provides the capability of using the register/latch as a buried state register/latch. The other eight macrocells have a single feedback path to the AND array. This feedback is user-selectable as either an I/O pin or a register/latch feedback (see Figure 2a).

Each macrocell can provide true input/output capability. The user can select each macrocell register/latch to be driven by either the signal generated by the AND-OR array or the I/O pin. When the I/O pin is selected as the input, the feedback path provides the register/latch input to the array. When used as an input, each macrocell is also user-programmable for registered, latched, or combinatorial input.

The PALCE29M16H has a dedicated CLK/$\overline{LE}$ pin and an I/CLK/$\overline{LE}$ pin. All macrocells have a programmable switch to choose between these two pins as the clock or latch enable signal. These signals are clock signals for macrocells configured as registers and latch enable signals for macrocells configured as latches. The polarity of these CLK/$\overline{LE}$ signals is also individually programmable. Thus different registers or latches can be driven by different clocks and clock phases.

The Output-Enable mode of each of the macrocells can be selected by the user. The I/O pin can be configured as an output pin (permanently enabled) or as an input pin (permanently disabled). It can also be configured as a dynamic I/O controlled by the Output Enable pin or by two AND-XOR product terms which are available for each bank of four I/O Logic Macrocells.

I/O Logic Macrocell Configuration

AMD's unique I/O macrocell offers major benefits through its versatile, programmable input/output cell structure, multiple clock choices, flexible Output Enable and feedback selection. Eight I/O macrocells with single feedback contain 9 EE cells, while the other eight macrocells contain 8 EE cells for programming the input/output functions (see Table 1).

EE cell S_1 controls whether the macrocell will be combinatorial or registered/latched. S_0 controls the output polarity (active-HIGH or active-LOW). S_2 determines whether the storage element is a register or a latch. S_3 allows the use of the macrocell as an input register/latch or as an output register/latch. It selects the direction of the data path through the register/latch. If connected to the usual AND-OR array output, the register/latch is an output connected to the I/O pin. If connected to the I/O pin, the register/latch becomes an input register/latch to the AND array using the feedback data path.

Programmable EE cells S_4 and S_5 allow the user to select one of the four CLK/$\overline{LE}$ signals for each macrocell. S_6 and S_7 are used to control Output Enable as pin controlled, two-product-term-controlled, permanently enabled or permanently disabled. S_8 controls a feedback multiplexer for the macrocells with a single feedback path only.

Using the programmable EE cells S_0–S_8 various input and output configurations can be selected. Some of the possible configuration options are shown in Figure 3.

In the unprogrammed state (charged, disconnected), an architectural cell is said to have a value of "1"; in the programmed state (discharged, connected to GND), an architectural cell is said to have a value of "0."

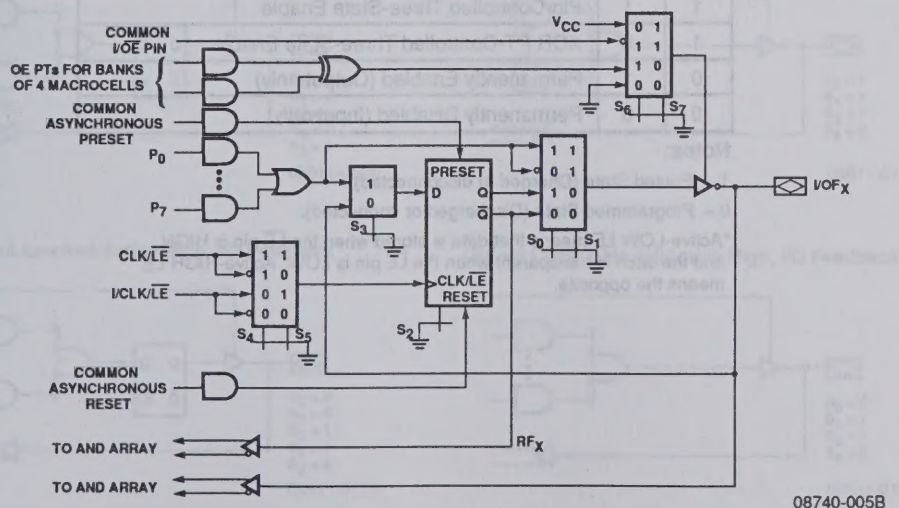


Figure 2b. PALCE29M16 Macrocell (Dual Feedback)

Table 1a. PALCE29M16 I/O Logic Macrocell Architecture Selections

S_3	I/O Cell
1	Output Cell
0	Input Cell

S_2	Storage Element
1	Register
0	Latch

S_1	Output Type
1	Combinatorial
0	Register/Latch

S_0	Output Polarity
1	Active LOW
0	Active HIGH

S_8	Feedback*
1	Combinatorial
0	Register/Latch

*Applies to macrocells with single feedback only.

Table 1b. PALCE29M16 I/O Logic Macrocell Clock Polarity and Output Enable Selections

S_4	S_5	Clock Edge/Latch Enable Level
1	1	CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE
1	0	CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE
0	1	I/CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE
0	0	I/CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE

S_6	S_7	Output Buffer Control
1	1	Pin-Controlled Three-State Enable
1	0	XOR PT-Controlled Three-State Enable
0	1	Permanently Enabled (Output only)
0	0	Permanently Disabled (Input only)

Notes:

1 = Erased State (Charged or disconnected).

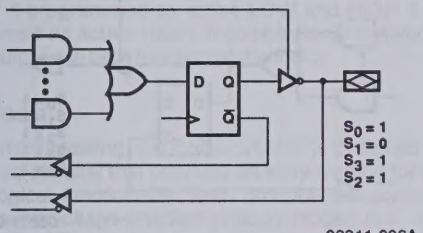
0 = Programmed State (Discharged or connected).

*Active-LOW LE means that data is stored when the $\overline{LE}$ pin is HIGH, and the latch is transparent when the $\overline{LE}$ pin is LOW. Active-HIGH LE means the opposite.

SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

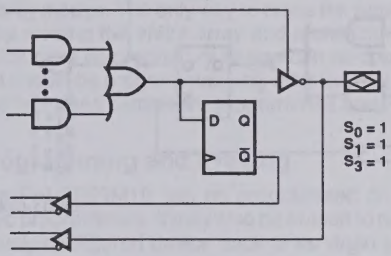
(For other useful configurations, please refer to the macrocell diagrams in Figure 2. All macrocell architecture cells are independently programmable).

Output Registered/Active Low



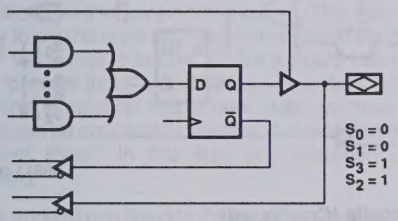
08811-006A

Output Combinatorial/Active Low



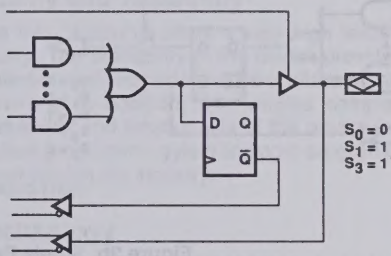
08811-007A

Output Registered/Active High



08811-008A

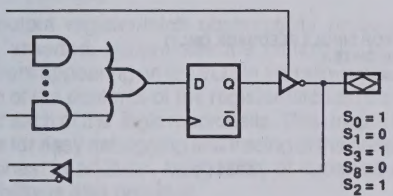
Output Combinatorial/Active High



08811-009A

Figure 3a. Dual Feedback Macrocells

Output Registered/Active Low, I/O Feedback



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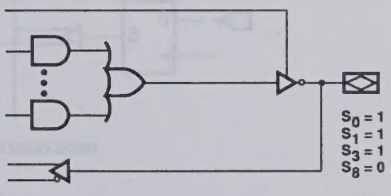
Output Combinatorial/Active Low, I/O Feedback



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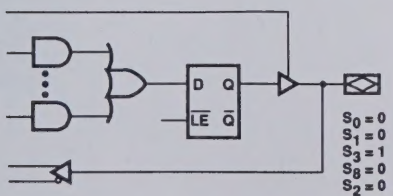
Output Latched/Active High, I/O Feedback



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Output Combinatorial/Active High, I/O Feedback

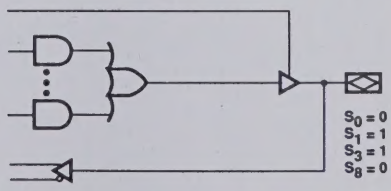

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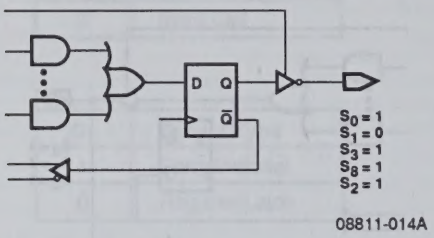
Figure 3b. Single Feedback Macrocells

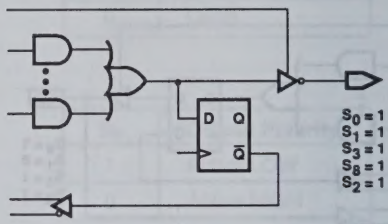
POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

Output Registered/Active Low, Register Feedback



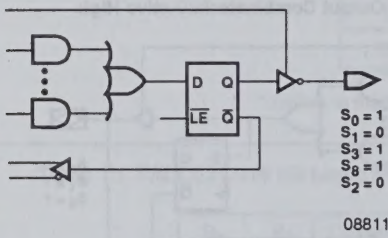
08811-014A

Output Combinatorial/Active Low, Register Feedback



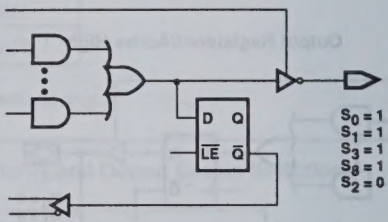
08811-015A

Output Latched/Active Low, Latched Feedback



08811-016A

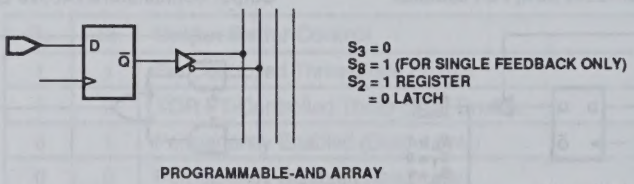
Output Combinatorial/Active Low, Latched Feedback



08811-017A

Figure 3b. Single Feedback Macrocells (Continued)

Input Registered/Latched



08811-018A

Figure 3c. All Macrocells

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. The outputs of the PALCE29M16 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW if programmed as active LOW and HIGH if programmed as active HIGH. If combinatorial is selected, the output will be a function of the logic.

Preload

To simplify testing, the PALCE29M16 is designed with preload circuitry that provides an easy method for testing logical functionality. Both product-term-controlled and supervoltage-enabled preload modes are available. The TTL-level preload product term can be useful during debugging, where supervoltages may not be available.

Preload allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device's inputs into an arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state," which can be checked to validate the transition from the "present state." In this way any transition can be checked.

Since preload can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

Observability

The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, preload, and the observability modes. The only way to erase the protection cell is by erasing the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

Programming and Erasing

The PALCE29M16 can be programmed on standard logic programmers. It may also be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erasure operation is required.

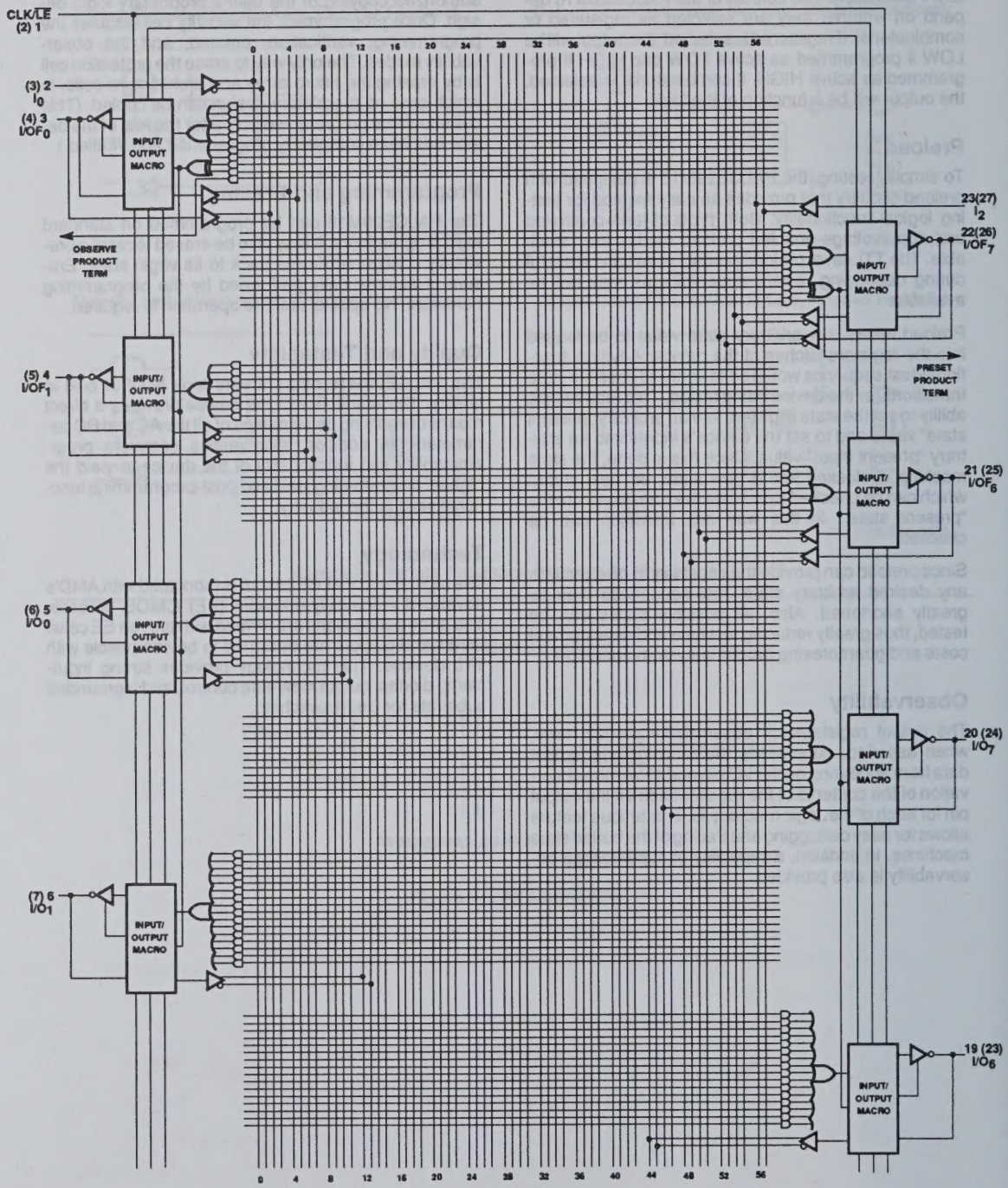
Quality and Testability

The PALCE29M16 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yield and post-programming functional yield in the industry.

Technology

The high-speed PALCE29M16 is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
DIP (PLCC) Pinouts



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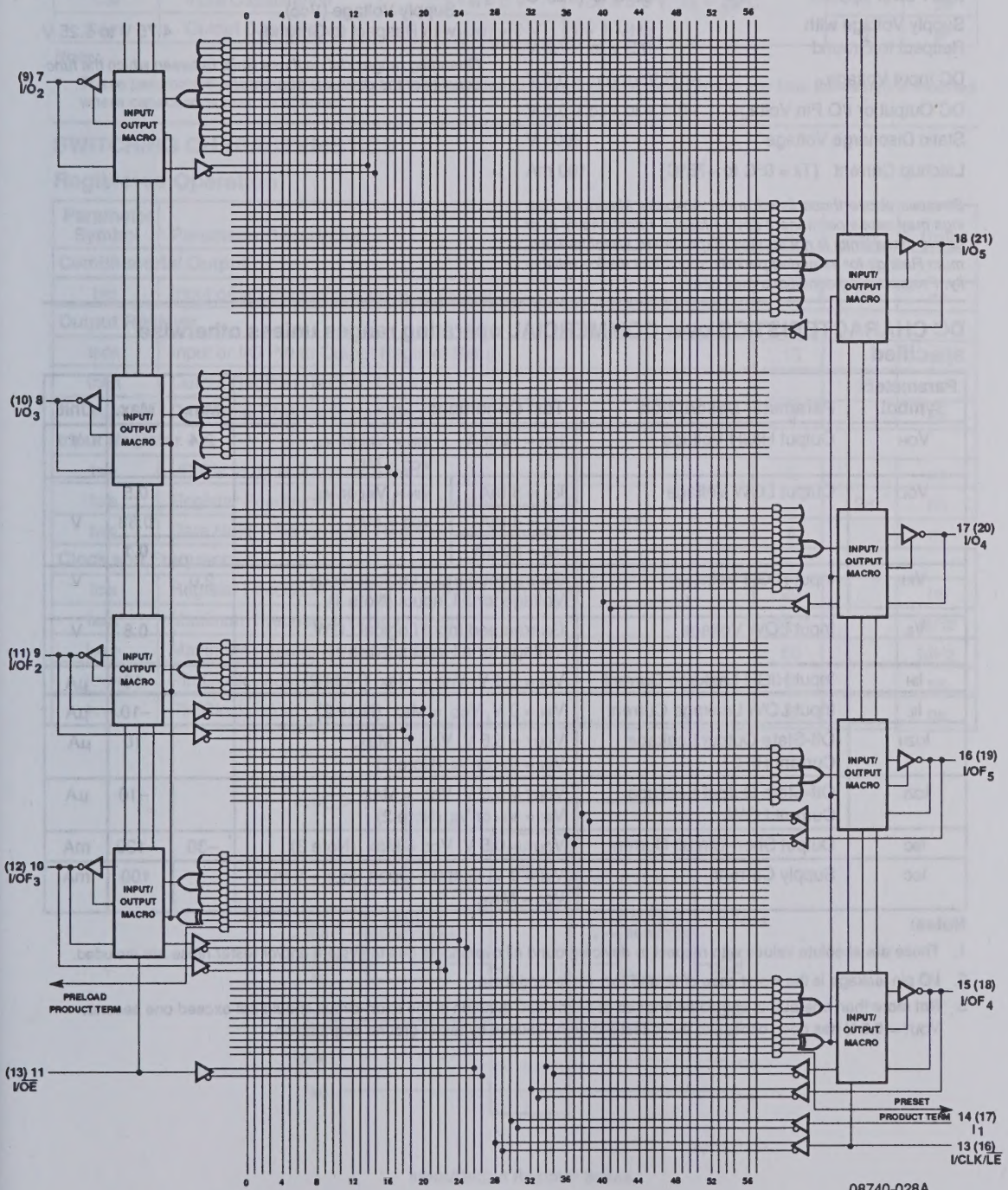
08740-028B

LOGIC DIAGRAM
DIP (PLCC) Pinouts

Continued From Previous Page



08740-028A
Concluded

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to 75°C
Supply Voltage (V_{CC}) with Respect to Ground	4.75 V to 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
		I_{OL} = 4 mA			0.33	
		I_{OL} = 20 µA			0.1	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			100	mA

Notes:

1. These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	f = 1 MHz	8	pF

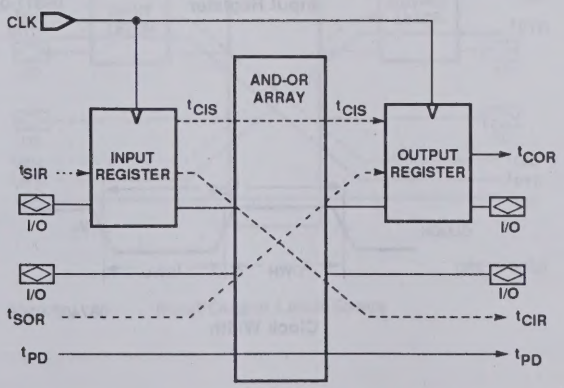
Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS

Registered Operation

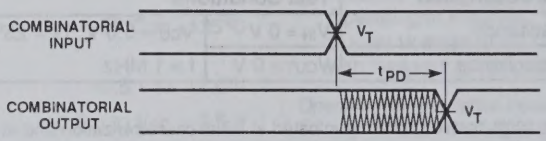
Parameter Symbol	Parameter Description	Min.	Max.	Unit
Combinatorial Output				
t_{PD}	Input or I/O Pin to Combinatorial Output		25	ns
Output Register				
t_{SOR}	Input or I/O Pin to Output Register Setup	15		ns
t_{COR}	Output Register Clock to Output		15	ns
t_{HOR}	Data Hold Time for Output Register	0		ns
Input Register				
t_{SIR}	I/O Pin to Input Register Setup	2		ns
t_{CIR}	Register Feedback Clock to Combinatorial Output		28	ns
t_{HIR}	Data Hold Time for Input Register	6		ns
Clock and Frequency				
t_{CIS}	Register Feedback to Output Register/Latch Setup	20		ns
f_{MAX}	Maximum Frequency 1/(t_{SOR} + t_{COR})	33.3		MHz
f_{MAXI}	Maximum Internal Frequency 1/t_{CIS}	50		MHz
t_{CWH}	Pin Clock Width HIGH	8		ns
t_{CWL}	Pin Clock Width LOW	8		ns



08811-020A

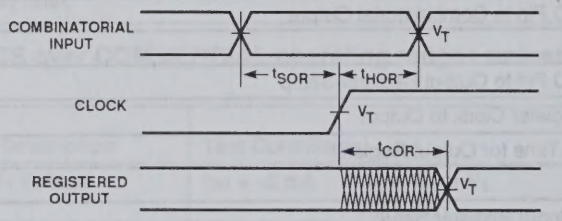
Input/Output Register Specs

SWITCHING WAVEFORMS



08811-022A

Combinatorial Output



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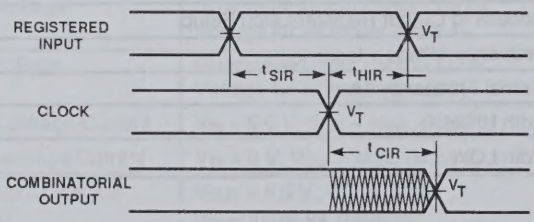
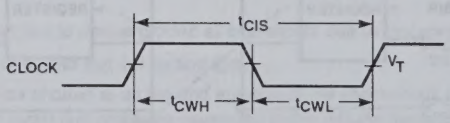
Output Register



Input Register

08811-024B



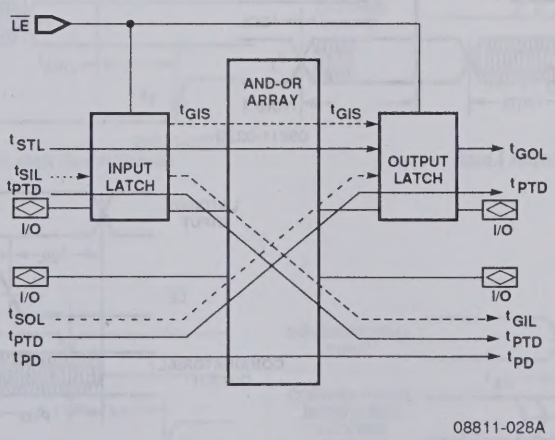
08740F-026B

Clock Width

SWITCHING CHARACTERISTICS

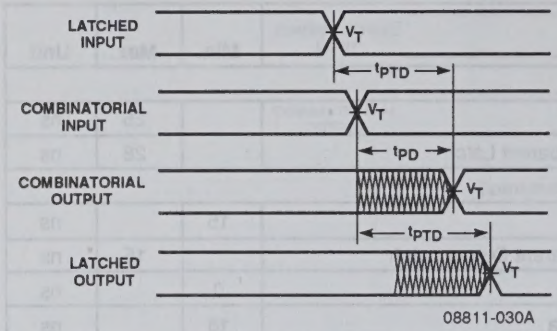
Latched Operation

Parameter Symbol	Parameter Description	Min.	Max.	Unit
Combinatorial Output				
t_{PD}	Input or I/O Pin to Combinatorial Output		25	ns
t_{PTD}	Input or I/O Pin to Output via One Transparent Latch		28	ns
Output Latch				
t_{SOL}	Input or I/O Pin to Output Latch Setup	15		ns
t_{GOL}	Latch Enable to Output Through Transparent Output Latch		15	ns
t_{HOL}	Data Hold Time for Output Latch	0		ns
t_{STL}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	18		ns
Input Latch				
t_{SIL}	I/O Pin to Input Latch Setup	2		ns
t_{GIL}	Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output		28	ns
t_{HIL}	Data Hold Time for Input Latch	6		ns
Latch Enable				
t_{GIS}	Latch Feedback to Output Register/Latch Setup	20		ns
t_{GWH}	Pin Enable Width HIGH	8		ns
t_{GWL}	Pin Enable Width LOW	8		ns

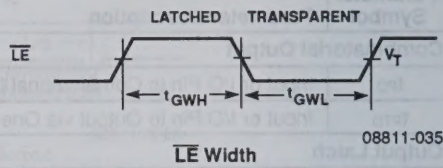


Input/Output Latch Specs

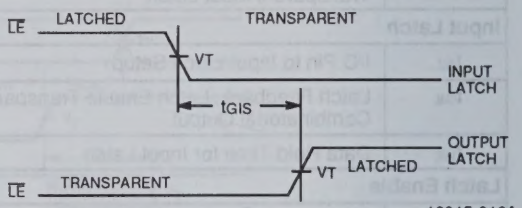
SWITCHING WAVEFORMS



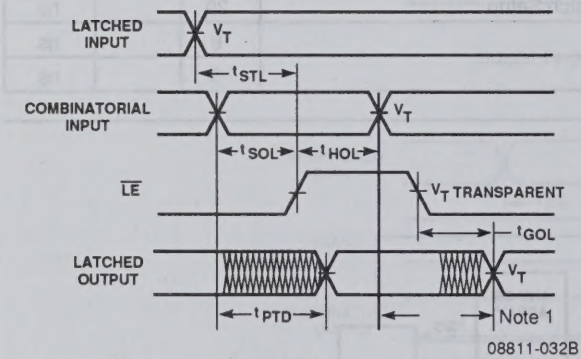
Latch (Transparent Mode)



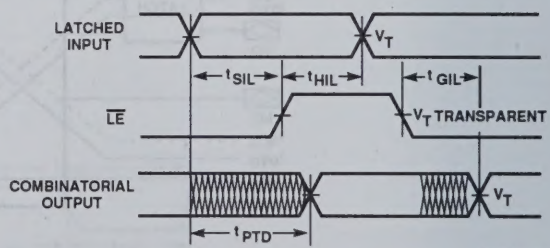
$\overline{LE}$ Width



Input and Output Latch Relationship



Output Latch



Note:

1. If the combinatorial input changes while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode after t_{PTD} ns has elapsed, the corresponding latched output will change t_{GOL} ns after $\overline{LE}$ goes into the transparent mode. If the combinatorial input change while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode before t_{PTD} ns has elapsed, the corresponding latched output will change at the later of the following – t_{PTD} ns after the combinatorial input changes or t_{GOL} ns after $\overline{LE}$ goes into the latched mode.

SWITCHING CHARACTERISTICS

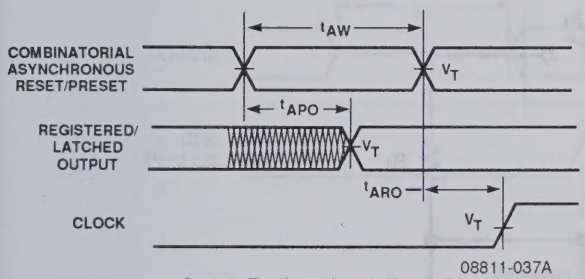
Reset/Preset, Enable

Parameter Symbol	Parameter Description	Min.	Max.	Unit
Combinatorial Output				
t_{APO}	Input or I/O Pin to Output Register/Latch Reset/Preset		30	ns
t_{AW}	Asynchronous Reset/Preset Pulse Width	15		ns
t_{ARO}	Asynchronous Reset/Preset to Output Register/Latch Recovery	15		ns
t_{ARI}	Asynchronous Reset/Preset to Input Register/Latch Recovery	12		ns
Output Enable Operation				
t_{PZX}	I/$\overline{OE}$ Pin to Output Enable		20	ns
t_{PXZ}	I/$\overline{OE}$ Pin to Output Disable (Note 1)		20	ns
t_{EA}	Input or I/O to Output Enable via PT		25	ns
t_{ER}	Input or I/O to Output Disable via PT (Note 1)		25	ns

Note:

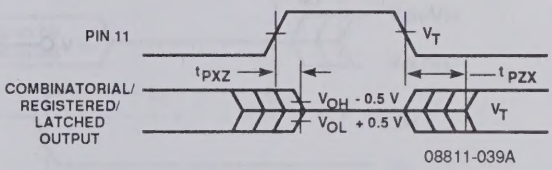
1. Output disable times do not include test load RC time constants.

SWITCHING WAVEFORMS



08811-037A

Output Register/Latch Reset/Preset



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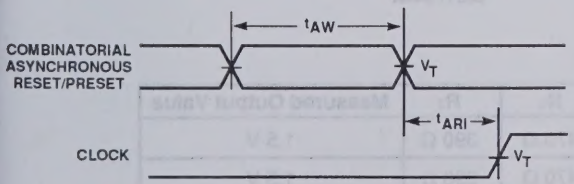
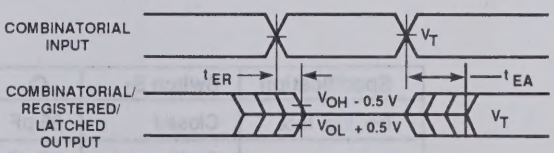
Pin 11 to Output Disable/Enable



08811-038A

Input Register/Latch Reset/Preset



08811-042A

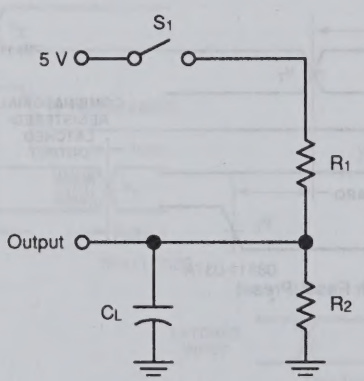
Input to Output Disable/Enable

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING TEST CIRCUIT



08811-044A

Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{GOL}	Closed	35 pF	470 Ω	390 Ω	1.5 V
t_{EA}, t_{PZX}	Z→H: open Z→L: closed	35 pF	470 Ω	390 Ω	1.5 V
t_{ER}, t_{PXZ}	H→Z: open L→Z: closed	5 pF	470 Ω	390 Ω	H→Z: V_{OH} –0.5 V L→Z: V_{OL} +0.5 V

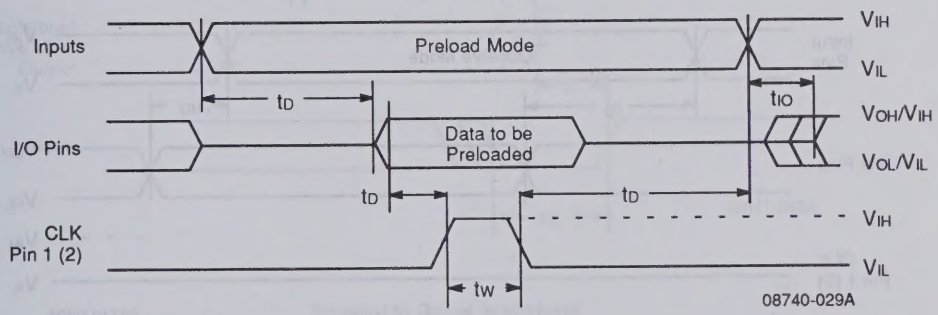
PRELOAD

The PALCE29M16 has the capability for product-term Preload. When the global-preload product term is true, the PALCE29M16 will enter the preload mode. This feature aids functional testing by allowing direct setting of register states. The procedure for Preload is as follows:

1. Set the selected input pins to the user selected preload condition.
2. Apply the desired register value to the I/O pins. This sets Q of the register. The value seen on the I/O pin, after Preload, will depend on whether the macrocell is active high or active low.
3. Pulse the clock pin (pin 1).
4. Remove the inputs to the I/O pins.
5. Remove the Preload condition.
6. Verify V_{OL}/V_{OH} for all output pins as per programmed pattern.

Because the Preload command is a product term, any input to the array can be used to set Preload (including I/O pins and registers). Preload itself will change the values of the I/O pins and registers. This will have unpredictable results. Therefore, only dedicated input pins should be used for the Preload command.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_D	Delay Time	0.5	1.0	5.0	µs
t_W	Pulse Width	250	500	700	ns
$t_{I/O}$	Valid Output	100		500	ns



Preload Waveform

OBSERVABILITY

The PALCE29M16 has the capability for product-term Observability. When the global-Observe product term is true, the PALCE29M16 will enter the Observe mode. This feature aids functional testing by allowing direct observation of register states.

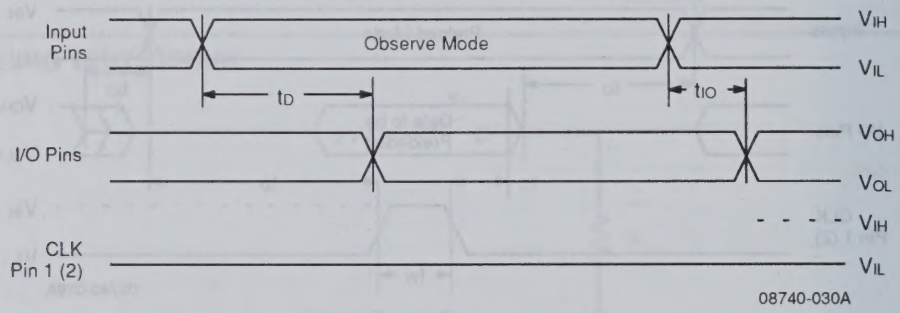
When the PALCE29M16 is in the Observe mode, the output buffer is enabled and the I/O pin value will be Q of the corresponding register. This overrides any $\overline{OE}$ inputs.

The procedure for Observe is:

1. Remove the inputs to all the I/O pins.
2. Set the inputs to the, user selected, Observe configuration.
3. The register values will be sent to the corresponding I/O pins.
4. Remove the Observe configuration from the selected I/O pins.

Because the Observe command is a product term, any input to the array can be used to set Observe (including I/O pins and registers). If I/O pins are used, the observe mode could cause a value change, which would cause the device to oscillate in and out of the Observe mode. Therefore, only dedicated input pins should be used for the Observe command.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_D	Delay Time	0.5	1.0	5.0	µs
$t_{I/O}$	Valid Output	100		500	ns



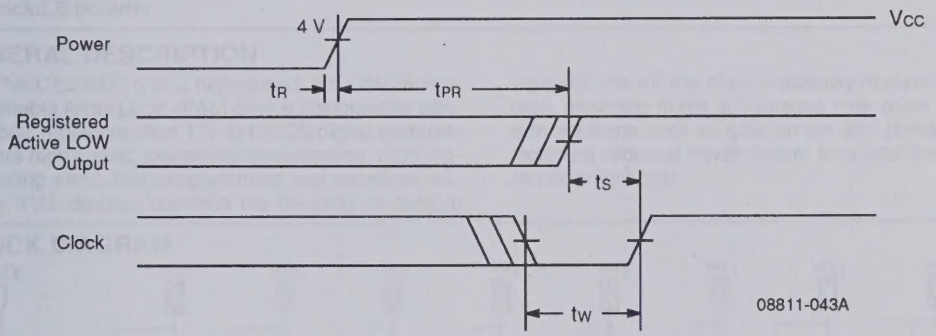
Observability Waveform

POWER-UP RESET

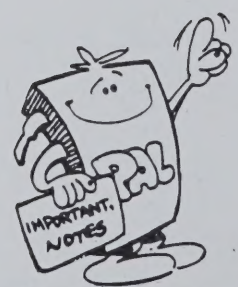
The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_W	Clock Width			
t_R	V_{CC} Rise Time	500		µs



Power-Up Reset Waveform


IMPORTANT
NOTES

PALCE29MA16H-25

24-Pin EE CMOS Programmable Array Logic

Advanced Micro Devices

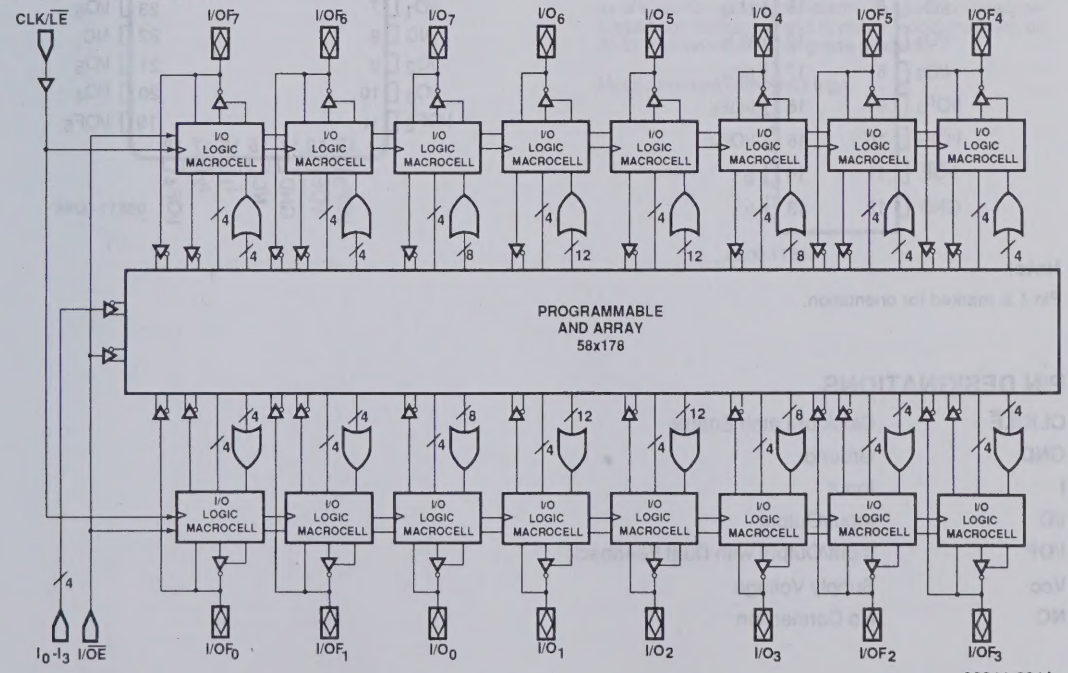
DISTINCTIVE CHARACTERISTICS

- High-performance semicustom logic replacement; Electrically Erasable (EE) technology allows reprogrammability
- 16 bidirectional user-programmable I/O logic macrocells for Combinatorial/Registered/ Latched operation
- Output Enable controlled by a pin or product terms
- Varied product term distribution for increased design flexibility
- Programmable clock selection with common pin clock/latch enable ($\overline{LE}$) or individual product term clock/$\overline{LE}$ with LOW/HIGH clock/$\overline{LE}$ polarity
- Register/Latch Preload permits full logic verification
- High speed (t_{PD} = 25 ns, f_{MAX} = 33 MHz and f_{MAX} internal = 50 MHz)
- Full-function AC and DC testing at the factory for high programming and functional yields and high reliability
- 24-pin 300-mil SKINNYDIP and 28-pin plastic leaded chip carrier packages
- Extensive third-party software and programmer support through FusionPLD partners

GENERAL DESCRIPTION

The PALCE29MA16 is a high-speed, EE CMOS Programmable Array Logic (PAL) device designed for general logic replacement in TTL or CMOS digital systems. It offers high speed, low power consumption, high programming yield, fast programming and excellent reliability. PAL devices combine the flexibility of custom logic with the off-the-shelf availability of standard products, providing major advantages over other semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.

BLOCK DIAGRAM



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Issue Date: January 1992

GENERAL DESCRIPTION (Continued)

The PALCE29MA16 uses the familiar sum-of-products (AND-OR) structure, allowing users to customize logic functions by programming the device for specific applications. It provides up to 29 array inputs and 16 outputs. It incorporates AMD's unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as combinatorial, registered, or latched with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the PALCE29MA16 by providing a varied number of logic product terms per output. Eight outputs have 4 product terms each, four outputs have 8 product terms each, and the other four outputs have 12 product terms each. This varied product-term distribution allows complex functions to be implemented in a single PAL device. Each output can be dynamically controlled by a common Output Enable pin or Output Enable product term. Each output can also be permanently enabled or disabled.

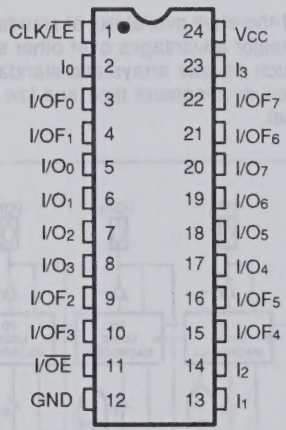
System operation has been enhanced by the addition of common asynchronous-Preset and Reset product terms and a power-up Reset feature. The PALCE29MA16 also incorporates Preload and Observability functions which permit full logic verification of the design.

The PALCE29MA16 is offered in the space-saving 300-mil SKINNYDIP package as well as the plastic leaded chip carrier package.

CONNECTION DIAGRAMS

Top View

SKINNYDIP



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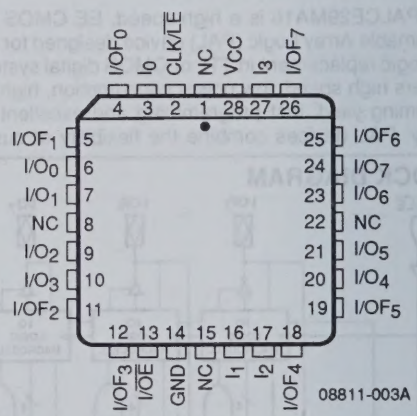
PLCC



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Note:

Pin 1 is marked for orientation.

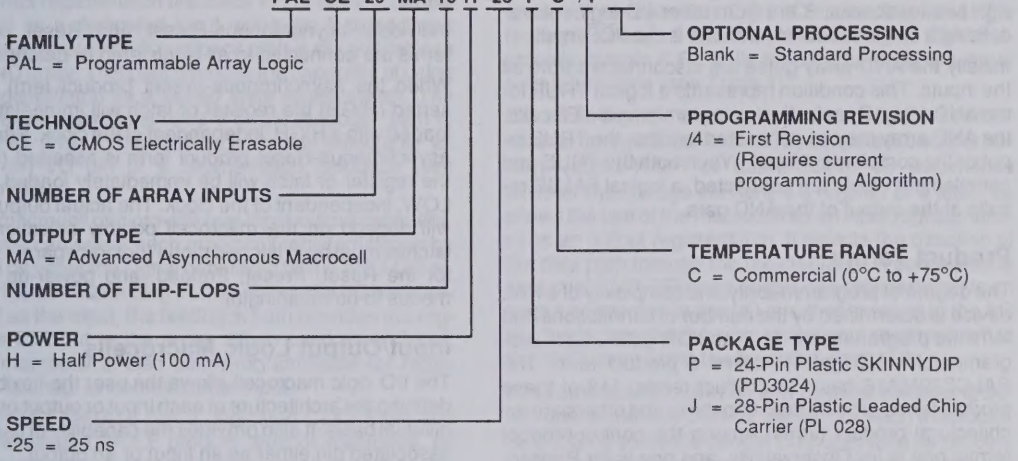
PIN DESIGNATIONS

CLK/$\overline{LE}$	Clock or Latch Enable
GND	Ground
I	Input
I/O	Input/Output
I/OF	Input/Output with Dual Feedback
V_{CC}	Supply Voltage
NC	No Connection

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:



Valid Combinations		
PALCE29MA16H-25	PC, JC	/4

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

Inputs

The PALCE29MA16 has 29 inputs to drive each product term (up to 58 inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram in Figure 1. Of these 29 inputs, 4 are dedicated inputs, 16 are from eight I/O logic macrocells with two feedbacks, 8 are from other I/O logic macrocells with single feedback and one is the I/$\overline{OE}$ input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE for the AND array. By selectively programming the EE cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The PALCE29MA16 has 178 product terms; 112 of these product terms provide logic capability and others are architectural product terms. Among the control product terms, one is for Observability, and one is for Preload. The Output Enable of each macrocell can be programmed to be controlled by a common Output Enable pin or an individual product term. It may also be permanently disabled. In addition, independent product terms for each macrocell control Preset, Reset and CLK/$\overline{LE}$.

Each product term on the PALCE29MA16 consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a varied distribution across the device ranging from 4 to 12 wide, with an average of 7 logic product terms per output. An increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

Individual asynchronous-Preset and Reset product terms are connected to all Registered or Latched I/Os.

When the asynchronous-Preset product term is asserted (HIGH) the register or latch will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-Reset product term is asserted (HIGH) the register or latch will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the Reset, Preset, Preload, and power-up Reset modes to be meaningful.

Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The PALCE29MA16 has 16 macrocells, one for each I/O pin. Each I/O macrocell can be programmed for combinatorial, registered or latched operation (see Figure 2). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers and Latches are used in synchronous logic applications. Registers and Latches with product term controlled clocks can also be used in asychronous application.

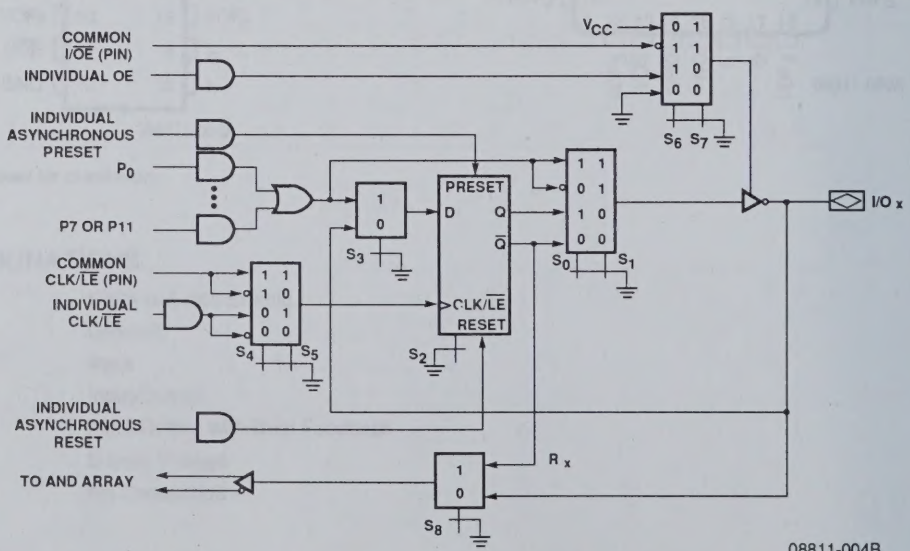


Figure 2a. PALCE29MA16 Macrocell (Single Feedback)

The output polarity for each macrocell in each of the three modes of operation is user-selectable, allowing complete flexibility of the macrocell configuration.

Eight of the macrocells (I/OF_0–I/OF_7) have two independent feedback paths to the AND array (see Figure 2b). The first is a dedicated I/O pin feedback to the AND array for combinatorial input. The second path consists of a direct register/latch feedback to the array. If the pin is used as a dedicated input using the first feedback path, the register/latch feedback path is still available to the AND array. This path provides the capability of using the register/latch as a buried state register/latch. The other eight macrocells have a single feedback path to the AND array. This feedback is user-selectable as either an I/O pin or a register/latch feedback (see Figure 2a).

Each macrocell can provide true input/output capability. The user can select each macrocell register/latch to be driven by either the signal generated by the AND-OR array or the corresponding I/O pin. When the I/O pin is selected as the input, the feedback path provides the register/latch input to the array. When used as an input, each macrocell is also user-programmable for registered, latched, or combinatorial input.

The PALCE29MA16 has a dedicated CLK/$\overline{LE}$ pin and one individual CLK/$\overline{LE}$ product term or macrocell. All macrocells have a programmable switch to choose between the CLK/$\overline{LE}$ pin and the CLK/$\overline{LE}$ product term as the clock or latch enable signal. These signals are clock signals for macrocells configured as registers and latch enable signals for macrocells configured as latches. The polarity of these CLK/$\overline{LE}$ signals is also individually programmable. Thus different registers or latches can be driven by different clocks and clock phases.

The Output-Enable mode of each of the macrocells can be selected by the user. The I/O pin can be configured as an output pin (permanently enabled) or as an input pin (permanently disabled). It can also be configured as a dynamic I/O controlled by the Output Enable pin or by a product term.

I/O Logic Macrocell Configuration

AMD's unique I/O macrocell offers major benefits through its versatile, programmable input/output cell structure, multiple clock choices, flexible Output Enable and feedback selection. Eight I/O macrocells with single feedback contain 9 EE cells, while the other eight macrocells contain 8 EE cells for programming the input/output functions (see Table 1).

EE cell S_1 controls whether the macrocell will be combinatorial or registered/latched. S_0 controls the output polarity (active-HIGH or active-LOW). S_2 determines whether the storage element is a register or a latch. S_3 allows the use of the macrocell as an input register/latch or as an output register/latch. It selects the direction of the data path through the register/latch. If connected to the usual AND-OR array output, the register/latch is an output connected to the I/O pin. If connected to the I/O pin, the register/latch becomes an input register/latch to the AND array using the feedback data path.

Programmable EE cells S_4 and S_5 allow the user to select one of the four CLK/$\overline{LE}$ signals for each macrocell. S_6 and S_7 are used to control Output Enable as pin controlled, product-term controlled, permanently enabled or permanently disabled. S_8 controls a feedback multiplexer for the macrocells with a single feedback path only.

Using the programmable EE cells S_0–S_8 various input and output configurations can be selected. Some of the possible configuration options are shown in Figure 3.

In the erased state (charged, disconnected), an architectural cell is said to have a value of "1"; in the programmed state (discharged, connected to GND), an architectural cell is said to have a value of "0."

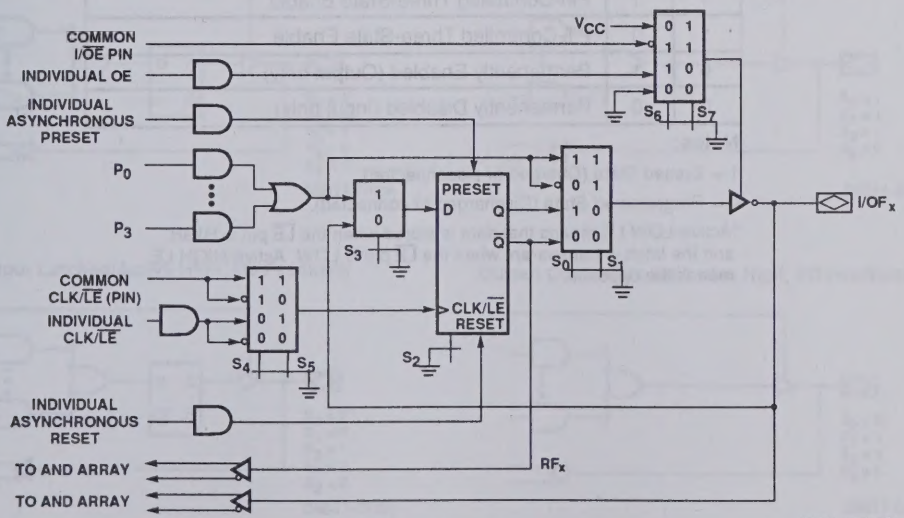


Figure 2b. PALCE29MA16 Macrocell (Dual Feedback)

Table 1a. PALCE29MA16 I/O Logic Macrocell Architecture Selections

S_3	I/O Cell
1	Output Cell
0	Input Cell

S_2	Storage Element
1	Register
0	Latch

S_1	Output Type
1	Combinatorial
0	Register/Latch

S_0	Output Polarity
1	Active LOW
0	Active HIGH

S_8	Feedback*
1	Register/Latch
0	I/O

*Applies to macrocells with single feedback only.

Table 1b. PALCE29MA16 I/O Logic Macrocell Clock Polarity and Output Enable Selections

S_4	S_5	Clock Edge/Latch Enable Level
1	1	CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE*
1	0	CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE*
0	1	CLK/$\overline{LE}$ PT positive-going edge, active-LOW LE*
0	0	CLK/$\overline{LE}$ PT negative-going edge, active-HIGH LE*

S_6	S_7	Output Buffer Control
1	1	Pin-Controlled Three-State Enable
1	0	PT-Controlled Three-State Enable
0	1	Permanently Enabled (Output only)
0	0	Permanently Disabled (Input only)

Notes:

1 = Erased State (Charged or disconnected).

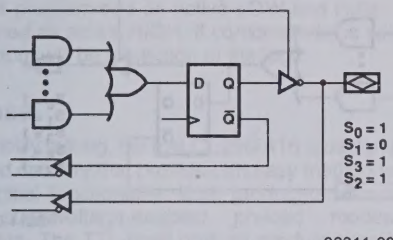
0 = Programmed State (Discharged or connected).

*Active-LOW LE means that data is stored when the $\overline{LE}$ pin is HIGH, and the latch is transparent when the $\overline{LE}$ pin is LOW. Active-HIGH LE means the opposite.

SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

(For other useful configurations, please refer to the macrocell diagrams in Figure 2. All macrocell architecture cells are independently programmable).

Output Registered/Active Low



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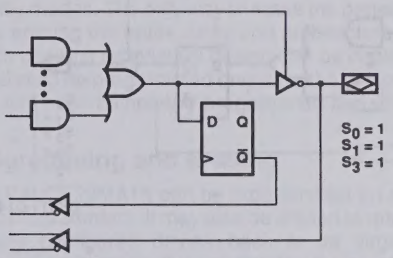
Output Combinatorial/Active Low



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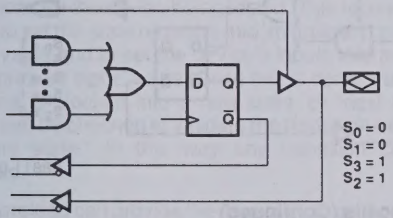
Output Registered/Active High



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Output Combinatorial/Active High

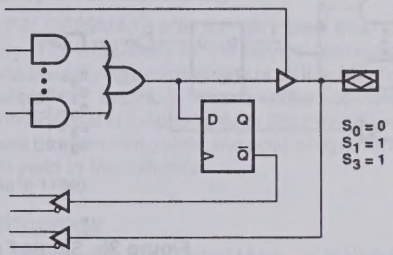

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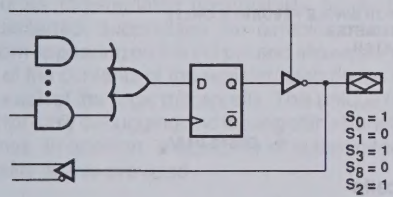
Figure 3a. Dual Feedback Macrocells

Output Registered/Active Low, I/O Feedback



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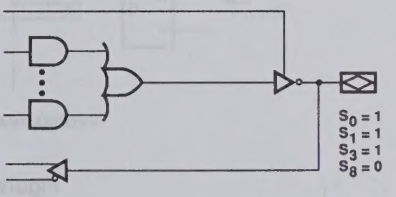
Output Combinatorial/Active Low, I/O Feedback



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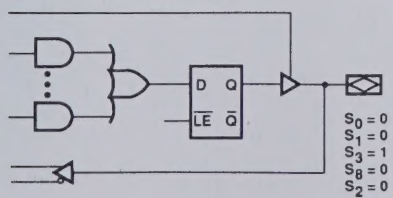
Output Latched/Active High, I/O Feedback



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Output Combinatorial/Active High, I/O Feedback

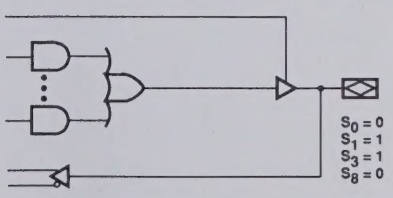

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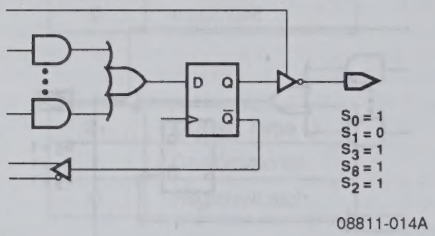
Figure 3b. Single Feedback Macrocells

SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

Output Registered/Active Low, Register Feedback



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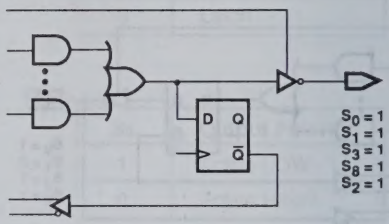
Output Combinatorial/Active Low, Register Feedback



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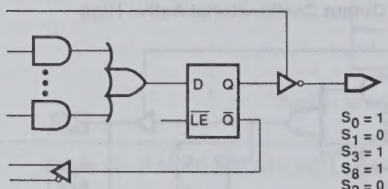
Output Latched/Active Low, Latched Feedback



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Output Combinatorial/Active Low, Latched Feedback

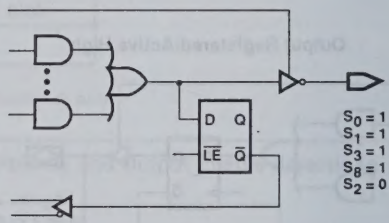

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Figure 3b. Single Feedback Macrocells (Continued)

Input Registered/Latched

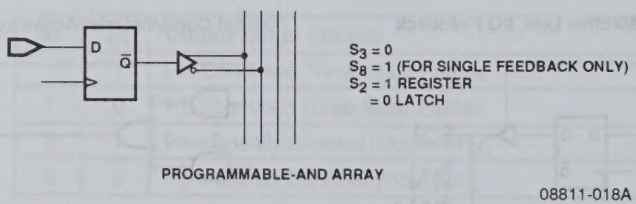

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Figure 3c. All Macrocells

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. The outputs of the PALCE29MA16 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW if programmed as active LOW and HIGH if programmed as active HIGH. If combinatorial is selected, the output will be a function of the logic.

Preload

To simplify testing, the PALCE29MA16 is designed with preload circuitry that provides an easy method for testing logical functionality. Both product-term-controlled and supervoltage-enabled preload modes are available. The TTL-level preload product term can be useful during debugging, where supervoltages may not be available.

Preload allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device's inputs into an arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state," which can be checked to validate the transition from the "present state." In this way any transition can be checked.

Since preload can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

Observability

The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, preload, and the observability modes. The only way to erase the protection cell is by erasing the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

Programming and Erasing

The PALCE29MA16 can be programmed on standard logic programmers. It may also be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erasure operation is required.

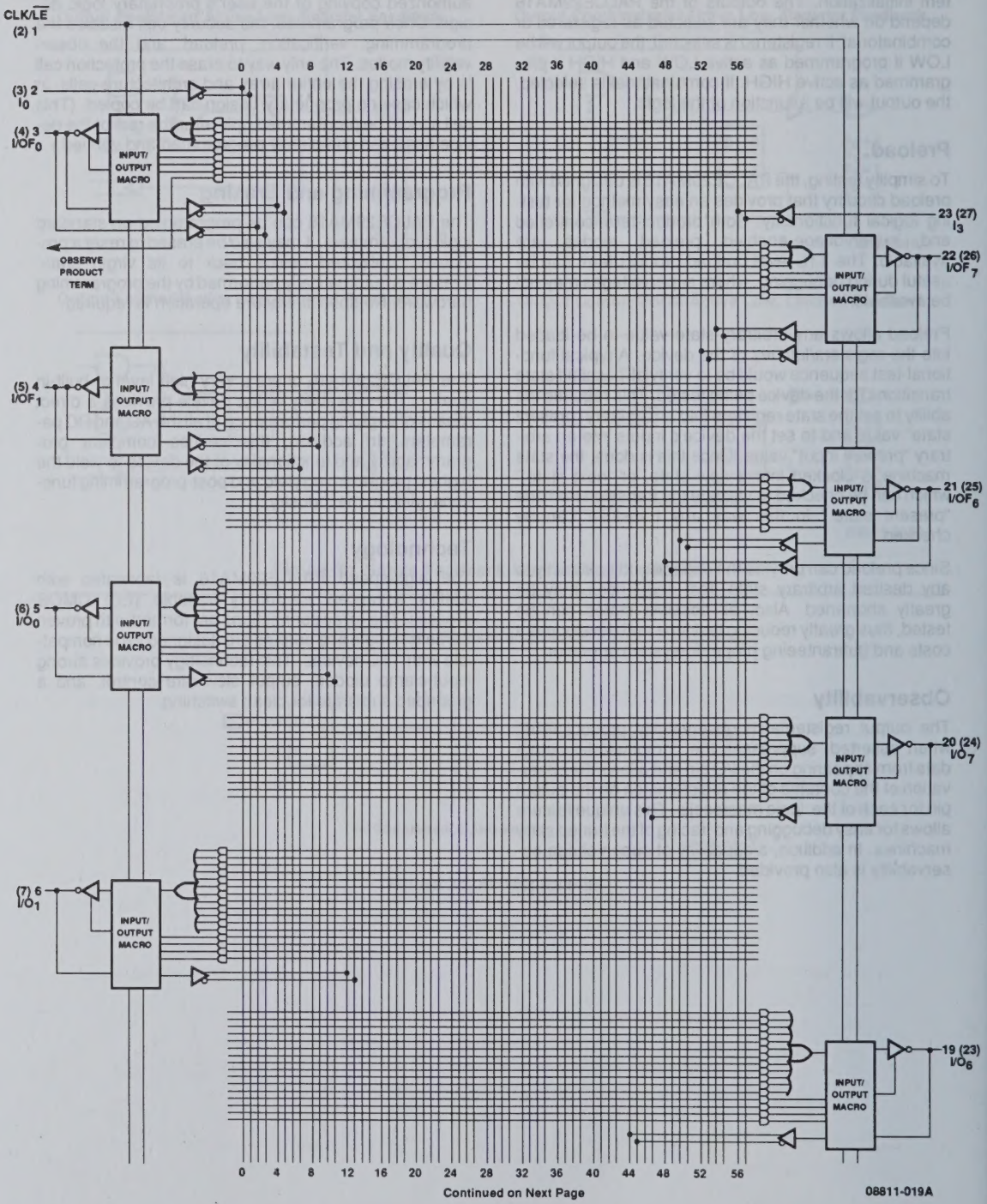
Quality and Testability

The PALCE29MA16 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yield and post-programming functional yield in the industry.

Technology

The high-speed PALCE29MA16 is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNY DIP (PLCC) Pinouts



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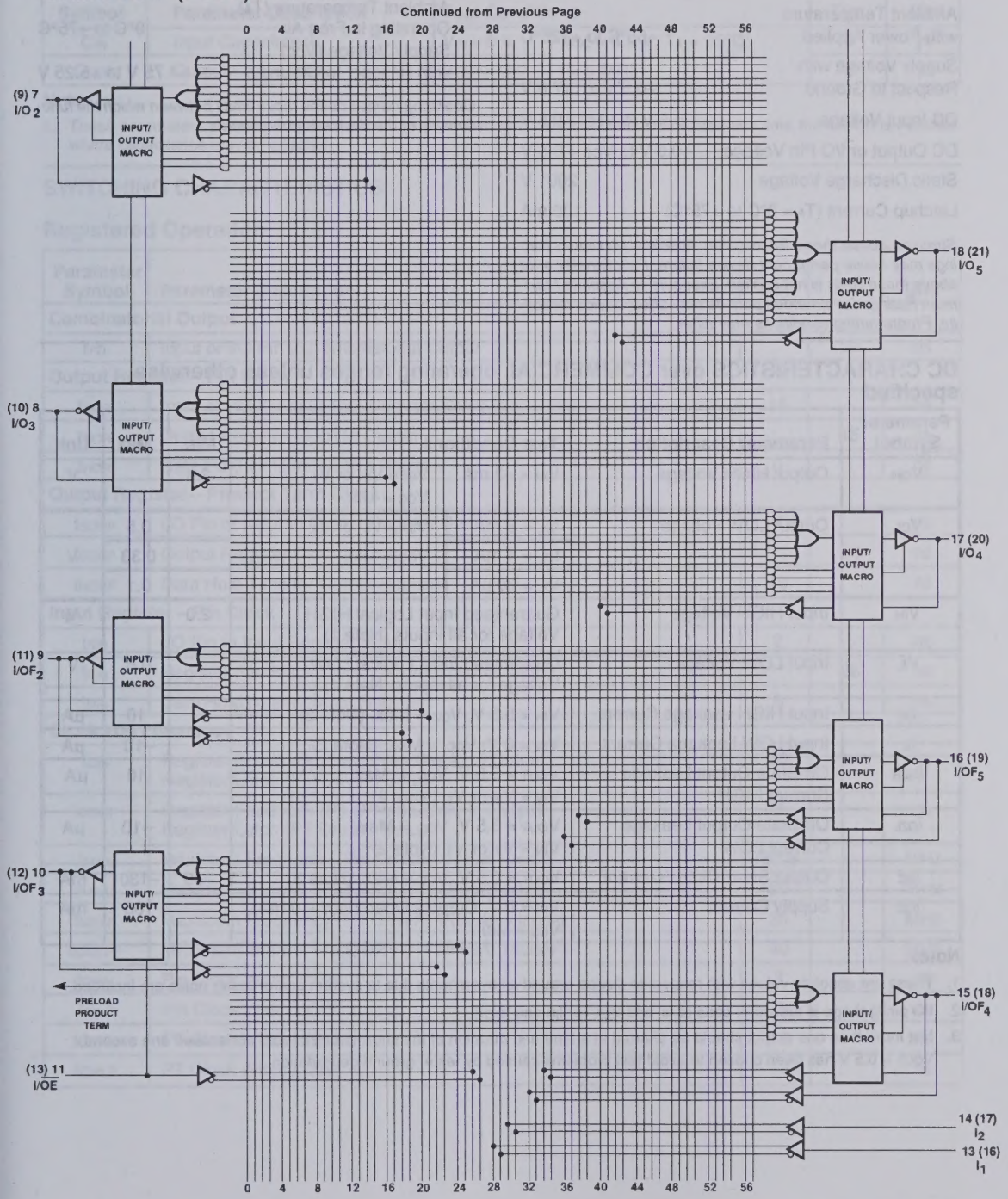
LOGIC DIAGRAM
SKINNY DIP (PLCC) Pinouts



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(Concluded)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
		I_{OL} = 4 mA			0.33	
		I_{OL} = 20 µA			0.1	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			100	mA

Notes:

1. These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	V_{CC} = 5.0 V, T_A = 25°C,	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	f = 1 MHz	8	pF

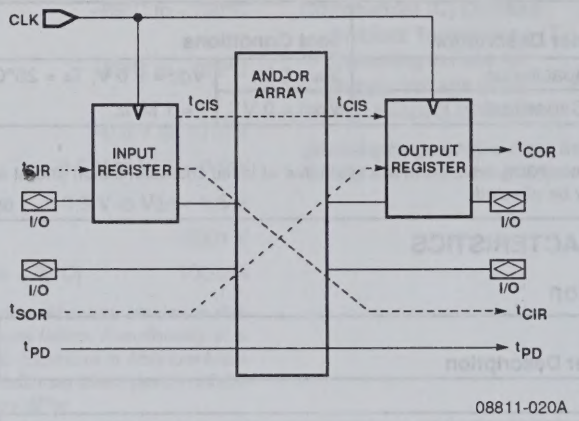
Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

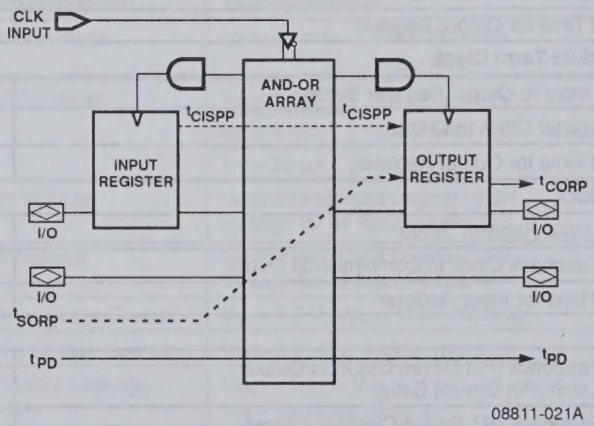
SWITCHING CHARACTERISTICS

Registered Operation

Parameter Symbol	Parameter Description	Min.	Max.	Unit
Combinatorial Output				
t_{PD}	Input or I/O Pin to Combinatorial Output		25	ns
Output Register – Pin Clock				
t_{SOR}	Input or I/O Pin to Output Register Setup	15		ns
t_{COR}	Output Register Clock to Output		15	ns
t_{HOR}	Data Hold Time for Output Register	0		ns
Output Register – Product Term Clock				
t_{SORP}	I/O Pin or Input to Output Register Setup	4		ns
t_{CORP}	Output Register Clock to Output		29	ns
t_{HORP}	Data Hold Time for Output Register	10		ns
Input Register – Pin Clock				
t_{SIR}	I/O Pin to Input Register Setup	2		ns
t_{CIR}	Register Feedback Clock to Combinatorial Output		28	ns
t_{HIR}	Data Hold time for Input Register	6		ns
Clock and Frequency				
t_{CIS}	Register Feedback (Pin Driven Clock) to Output Register/Latch (Pin Driven) Setup	20		ns
t_{CISPP}	Register Feedback (PT Driven Clock) to Output Register/Latch (PT Driven) Setup	25		ns
f_{MAX}	Maximum Frequency (Pin Driven) $1/(t_{SOR} + t_{COR})$	33.3		MHz
f_{MAXI}	Maximum Internal Frequency (Pin Driven) $1/t_{CIS}$	50		MHz
f_{MAXP}	Maximum Frequency (PT Driven) $1/(t_{SORP} + t_{CORP})$	30		MHz
f_{MAXIPP}	Maximum Internal Frequency (PT Driven) $1/t_{CISPP}$	40		MHz
t_{CWH}	Pin Clock Width HIGH	8		ns
t_{CWL}	Pin Clock Width LOW	8		ns
t_{CWHP}	PT Clock Width HIGH	12		ns
t_{CWLP}	PT Clock Width LOW	12		ns

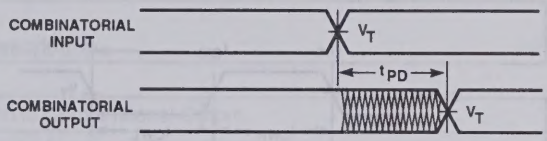


Input/Output Register Specs (Pin CLK Reference)



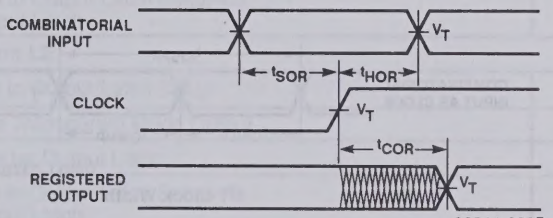
Input/Output Register Specs (PT CLK Reference)

SWITCHING WAVEFORMS



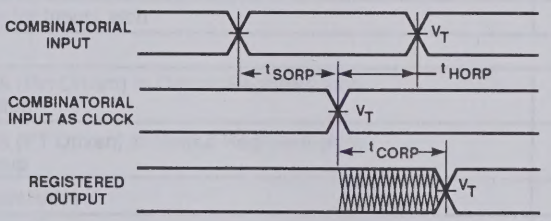
08811-022A

Combinatorial Output



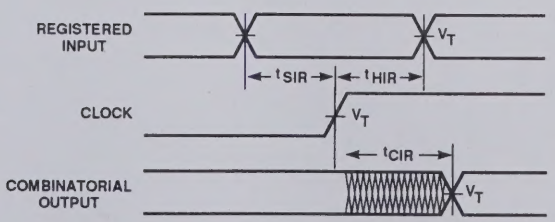
08811-023B

Output Register (Pin Clock)



08811-024B

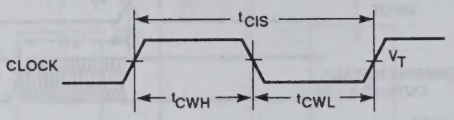
Output Register (PT Clock)



08811-025B

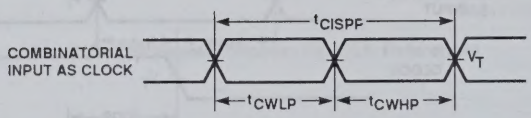
Input Register

SWITCHING WAVEFORMS



08811-026B

Pin Clock Width



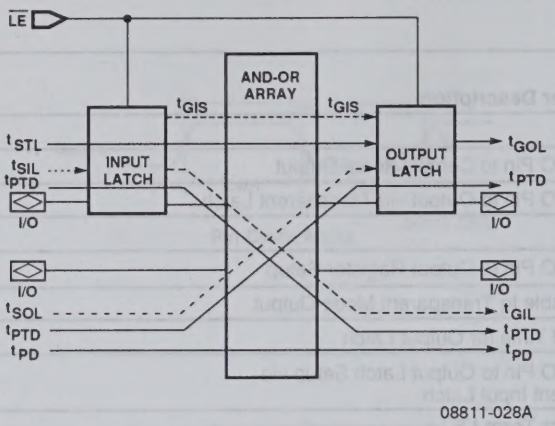
08811-027B

PT Clock Width

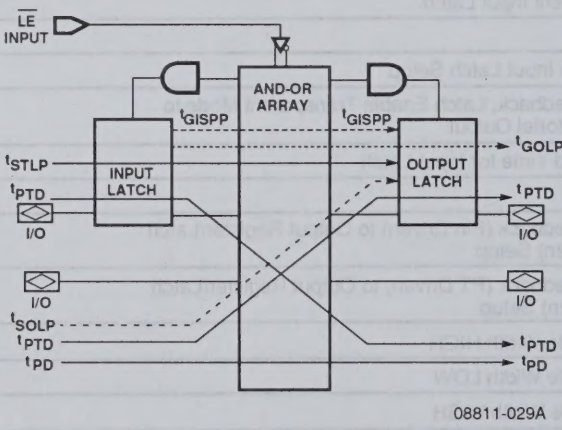
SWITCHING CHARACTERISTICS

Latched Operation

Parameter Symbol	Parameter Description	Min.	Max.	Unit
Combinatorial Output				
t_{PD}	Input or I/O Pin to Combinatorial Output		25	ns
t_{PTD}	Input or I/O Pin to Output via Transparent Latch		28	ns
Output Latch – Pin LE				
t_{SOL}	Input or I/O Pin to Output Register Setup	15		ns
t_{GOL}	Latch Enable to Transparent Mode Output		15	ns
t_{HOL}	Data Hold Time for Output Latch	0		ns
t_{STL}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	18		ns
Output Latch – Product Term LE				
t_{SOLP}	Input or I/O Pin to Output Latch Setup	4		ns
t_{GOLP}	Latch Enable to Transparent Mode Output		29	ns
t_{HOLP}	Data Hold Time for Output Latch	10		ns
t_{STLP}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	10		ns
Input Latch – Pin LE				
t_{SIL}	I/O Pin to Input Latch Setup	2		ns
t_{GIL}	Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output		28	ns
t_{HIL}	Data Hold Time for Input Latch	6		ns
Latch Enable				
t_{GIS}	Latch Feedback (Pin Driven) to Output Register/Latch (Pin Driven) Setup	20		ns
t_{GISPP}	Latch Feedback (PT Driven) to Output Register/Latch (PT Driven) Setup	25		ns
t_{GWH}	Pin Enable Width HIGH	8		ns
t_{GWL}	Pin Enable Width LOW	8		ns
t_{GWHP}	PT Enable Width HIGH	12		ns
t_{GWLP}	PT Enable Width LOW	12		ns

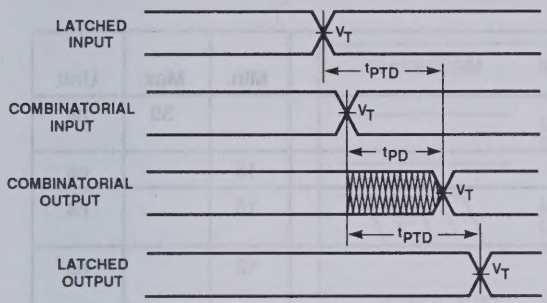


Input/Output Latch Specs (Pin $\overline{LE}$ Reference)



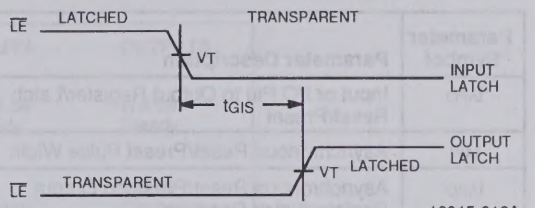
Input/Output Latch Specs (PT $\overline{LE}$ Reference)

SWITCHING WAVEFORMS



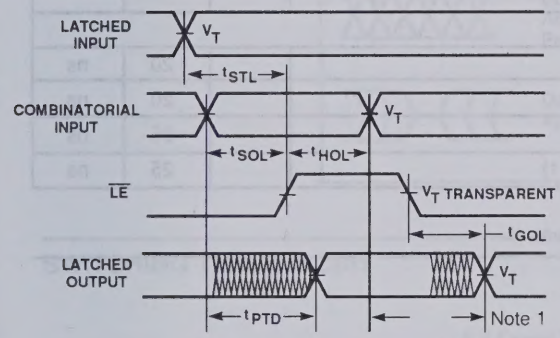
08811-030A

Latch (Transparent Mode)



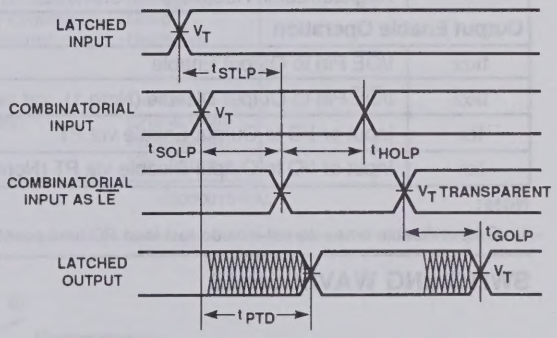
12015-012A

Input and Output Latch Relationship



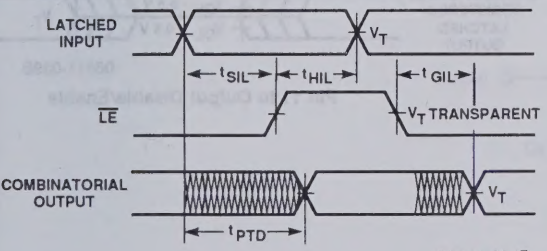
08811-032B

Output Latch (Pin $\overline{LE}$)



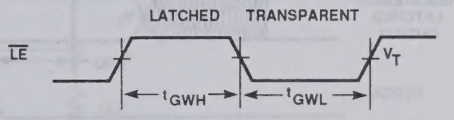
08811-033B

Output Latch (PT $\overline{LE}$)



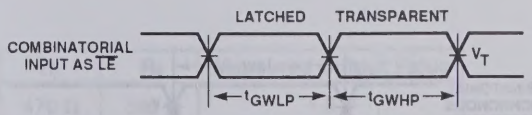
08811-034B

Input Latch (Pin $\overline{LE}$)



08811-035B

Pin $\overline{LE}$ Width



08811-036B

PT $\overline{LE}$ Width

Note:

1. If the combinatorial input changes while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode after t_{PTD} ns has elasped, the corresponding latched output will change t_{GOL} ns after $\overline{LE}$ goes into the transparent mode. If the combinatorial input changes while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode before t_{PTD} ns has elapsed, the corresponding latched output will change at the later of the following – t_{PTD} ns after the combinatorial input changes or t_{GOL} ns after $\overline{LE}$ goes into the latched mode.

SWITCHING CHARACTERISTICS

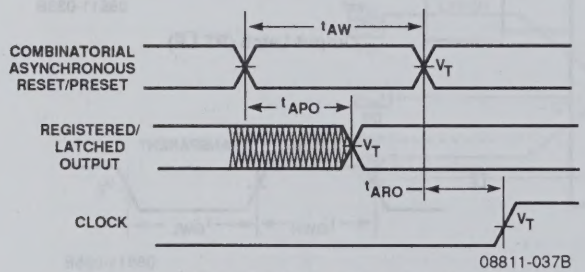
Reset/Preset, Enable

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{APO}	Input or I/O Pin to Output Register/Latch Reset/Preset		30	ns
t_{AW}	Asynchronous Reset/Preset Pulse Width	15		ns
t_{ARO}	Asynchronous Reset/Preset to Output Register/Latch Recovery	15		ns
t_{ARI}	Asynchronous Reset/Preset to Input Register/Latch Recovery	12		ns
t_{ARPO}	Asynchronous Reset/Preset to Output Register/Latch Recovery PT Clock/LE	4		ns
t_{ARPI}	Asynchronous Reset/Preset to Input Register/Latch Recovery PT Clock/LE	6		ns
Output Enable Operation				
t_{PZX}	I/$\overline{OE}$ Pin to Output Enable		20	ns
t_{PXZ}	I/$\overline{OE}$ Pin to Output Disable (Note 1)		20	ns
t_{EA}	Input or I/O to Output Enable via PT		25	ns
t_{ER}	Input or I/O to Output Disable via PT (Note 1)		25	ns

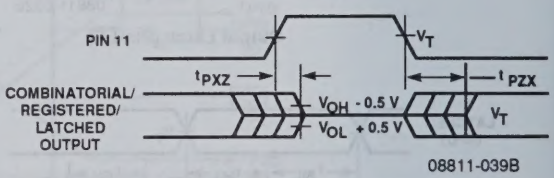
Note:

1. Output disable times do not include test load RC time constants.

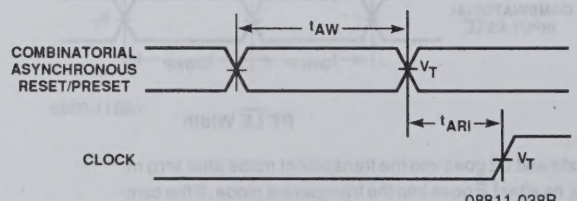
SWITCHING WAVEFORMS



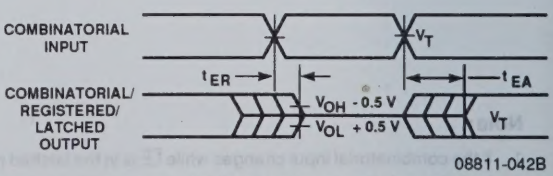
Output Register/Latch Reset/Preset



Pin 11 to Output Disable/Enable



Input Register/Latch Reset/Preset



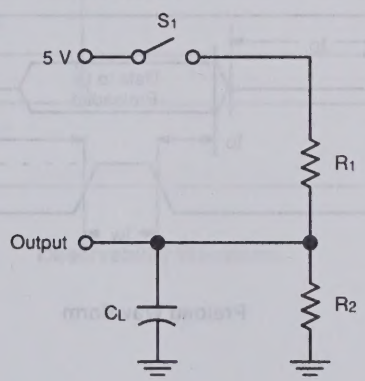
Input to Output Disable/Enable

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



08811-044A

Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{GOL}	Closed	35 pF	470 Ω	390 Ω	1.5 V
t_{EA}, t_{PZX}	Z→H: open Z→L: closed	35 pF	470 Ω	390 Ω	1.5 V
t_{ER}, t_{PXZ}	H→Z: open L→Z: closed	5 pF	470 Ω	390 Ω	H→Z: V_{OH} –0.5 V L→Z: V_{OL} +0.5 V

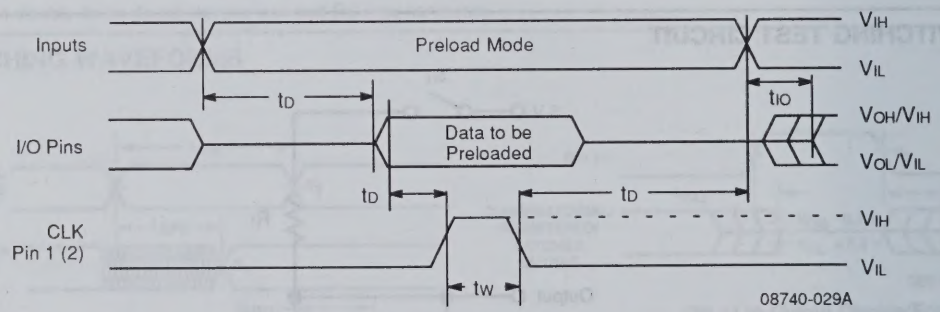
PRELOAD

The PALCE29MA16 has the capability for product-term Preload. When the global-preload product term is true, the PALCE29MA16 will enter the preload mode. This feature aids functional testing by allowing direct setting of register states. The procedure for Preload is as follows:

1. Set the selected input pins to the user selected preload condition.
2. Apply the desired register value to the I/O pins. This sets Q of the register. The value seen on the I/O pin, after Preload, will depend on whether the macrocell is active high or active low.
3. Pulse the clock pin (pin 1).
4. Remove the inputs to the I/O pins.
5. Remove the Preload condition.
6. Verify V_{OL}/V_{OH} for all output pins as per programmed pattern.

Because the Preload command is a product term, any input to the array can be used to set Preload (including I/O pins and registers). Preload itself will change the values of the I/O pins and registers. This will have unpredictable results. Therefore, only dedicated input pins should be used for the Preload command.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_D	Delay Time	0.5	1.0	5.0	µs
tw	Pulse Width	250	500	700	ns
$t_{I/O}$	Valid Output	100		500	ns



Preload Waveform

OBSERVABILITY

The PALCE29MA16 has the capability for product-term Observability. When the global-Observe product term is true, the PALCE29MA16 will enter the Observe mode. This feature aids functional testing by allowing direct observation of register states.

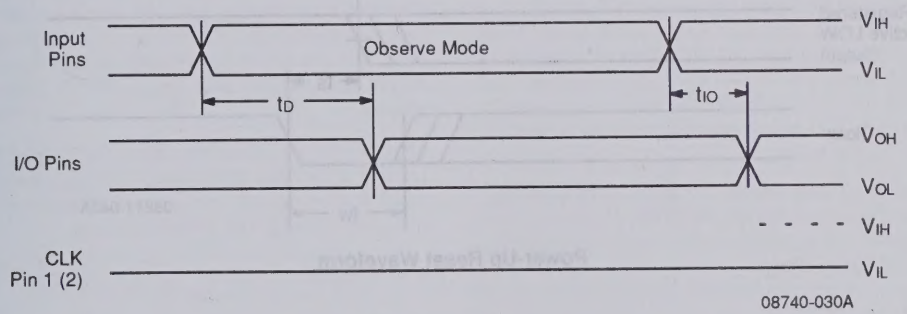
When the PALCE29MA16 is in the Observe mode, the output buffer is enabled and the I/O pin value will be Q of the corresponding register. This overrides any $\overline{OE}$ inputs.

The procedure for Observe is:

1. Remove the inputs to all the I/O pins.
2. Set the inputs to the, user selected, Observe configuration.
3. The register values will be sent to the corresponding I/O pins.
4. Remove the Observe configuration from the selected I/O pins.

Because the Observe command is a product term, any input to the array can be used to set Observe (including I/O pins and registers). If I/O pins are used, the observe mode could cause a value change, which would cause the device to oscillate in and out of the Observe mode. Therefore, only dedicated input pins should be used for the Observe command.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_D	Delay Time	0.5	1.0	5.0	µs
$t_{I/O}$	Valid Output	100		500	ns



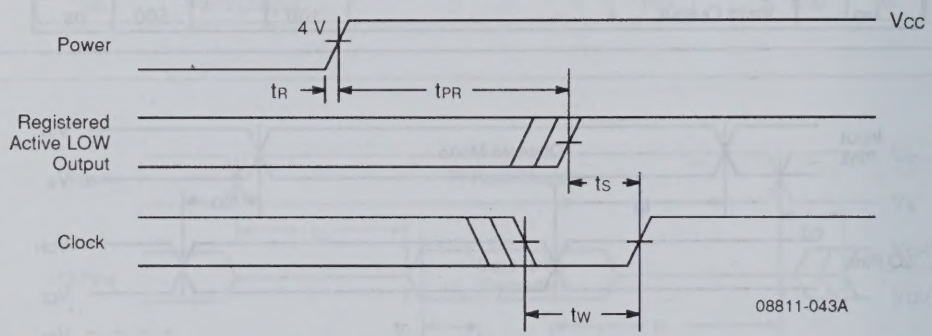
Observability Waveform

POWER-UP RESET

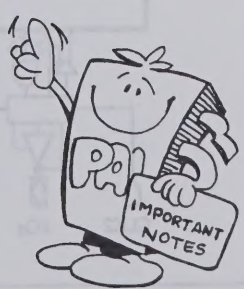
The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_W	Clock Width			
t_R	V_{CC} Rise Time	500		µs



Power-Up Reset Waveform


IMPORTANT
NOTES

PALCE610 Family

EE CMOS High Performance Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- AMD's Programmable Array Logic (PAL) architecture
- Electrically-erasable CMOS technology providing half power (90 mA I_{CC}) at high speed
  -15 = 15 ns t_{PD}
  -25 = 25 ns t_{PD}
- Sixteen macrocells with configurable I/O architecture
- Registered or combinatorial operation
- Registers programmable as D, T, J–K, or S–R
- Asynchronous clocking via product term or bank register clocking from external pins
- Register preload for testability
- Power-up reset for initialization
- Space-saving 24-pin SKINNYDIP and 28-pin PLCC packages
- Fully tested for 100% programming yield and high reliability
- Extensive third–party software and programmer support through FusionPLD partners

GENERAL DESCRIPTION

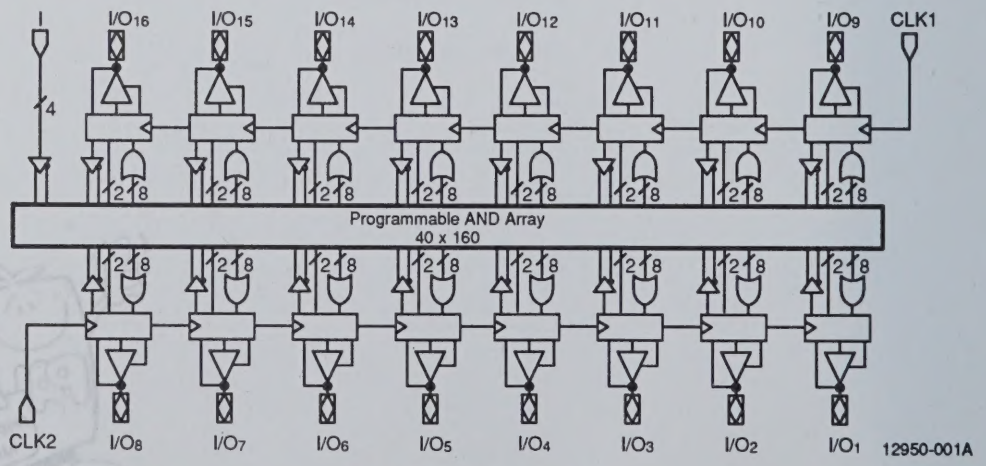
The PALCE610 is a general purpose PAL device and is functionally and fuse map equivalent to the EP610. It can accommodate logic functions with up to 20 inputs and 16 outputs. There are 16 I/O macrocells that can be individually configured to the user's specifications. The macrocells can be configured as either registered or combinatorial. The registers can be configured as D, T, J–K, or S–R flip-flops.

The PALCE610 uses the familiar sum-of-products logic with programmable-AND and fixed-OR structure. Eight product terms are brought to each macrocell to provide logic implementations.

The PALCE610 is manufactured using advanced CMOS EE technology providing high density and low power consumption. Moreover, it is a high-speed device having a worst-case t_{PD} of 15 ns. Space-saving 24-pin SKINNYDIP and 28-pin PLCC packages are offered.

This device can be quickly erased and reprogrammed providing for easy prototyping. Once a device is programmed the security bit can be used to provide protection from copying a proprietary design.

BLOCK DIAGRAM

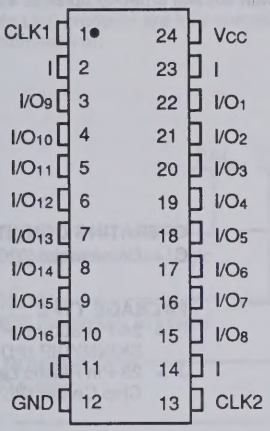


Publication # 12950 Rev. E Amendment /0
Issue Date: January 1992

CONNECTION DIAGRAMS

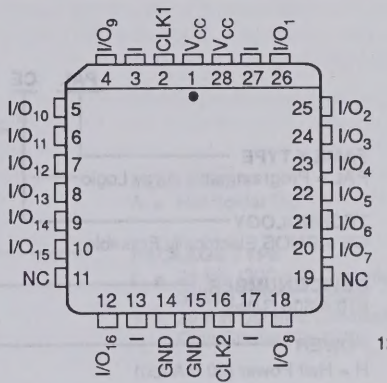
Top View

SKINNYDIP



12950-002A

PLCC/LCC



12950-003A

Note:
Pin 1 is marked for orientation

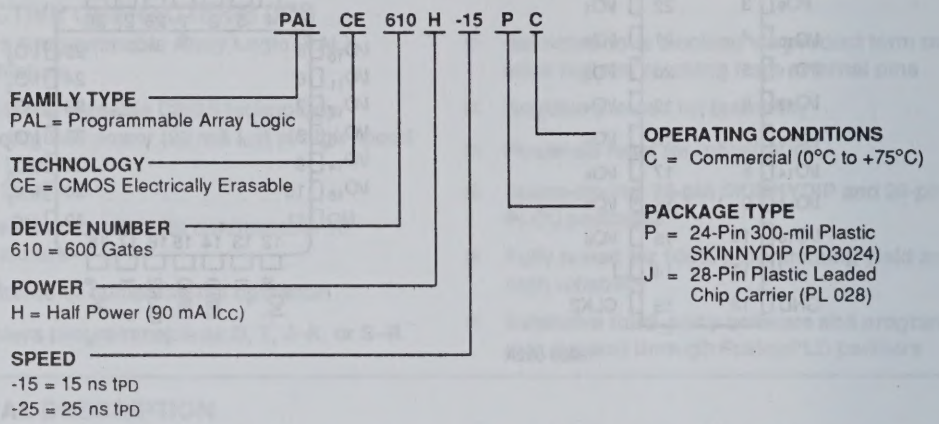
PIN DESIGNATIONS

CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
Vcc	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE610H-15	PC, JC
PALCE610H-25	

Valid Combinations

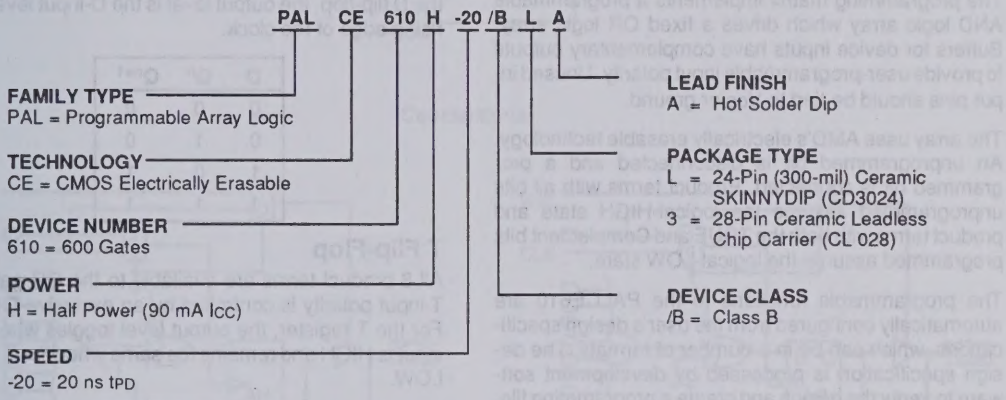
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE610H-20	/BLA,/B3A

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-in

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PALCE610 is a general purpose programmable logic device. It has 16 independently-configurable macrocells. Each macrocell can be configured as either combinatorial or registered. The registers can be D, T, J–K, or S–R type flip-flops. The device has 4 dedicated input pins and 2 clock pins. Each clock pin controls 8 of the 16 macrocells.

The programming matrix implements a programmable AND logic array which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input polarity. Unused input pins should be tied to V_{CC} or ground.

The array uses AMD's electrically erasable technology. An unprogrammed bit is disconnected and a programmed bit is connected. Product terms with all bits unprogrammed assume the logical-HIGH state and product terms with both the TRUE and Complement bits programmed assume the logical-LOW state.

The programmable functions in the PALCE610 are automatically configured from the user's design specifications, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to the programmer, configures the design according to the user's desired function.

Macrocell Configurations

The PALCE610 macrocell can be configured as either combinatorial or registered. Both the combinatorial and registered configurations have output polarity control. The register can be configured as a D, T, J–K, or S–R type flip-flop. Figure 1 shows the possible configurations.

Each macrocell can select as its clock either the corresponding clock pin or the CLK/OE product term. If the clock pin is selected, the output enable is controlled by the CLK/OE product term. If the CLK/OE product term is selected, the output is always enabled.

Combinatorial I/O

All 8 product terms are available to the OR gate. The output-enable function is performed by the CLK/OE product term.

Registered Configurations

There are 4 flip-flop types available: D, T, J–K and S–R.

The registers can be configured as synchronous or asynchronous. In the synchronous configuration, the clock is controlled by the clock input pin. The output enable is controlled by the product term function. In the asynchronous configuration, the clock input is controlled by the product term. The output is always enabled.

In The D and T configurations, feedback can be either from Q or the output pin. This allows D and T configurations to be either outputs or I/O. In the J–K and S–R configurations, feedback is only from Q; therefore, J–K and S–R configurations are strictly outputs.

D Flip-Flop

All 8 product terms are available to the OR gate. The D input polarity is controlled by an exclusive-OR gate. For the D flip-flop, the output level is the D-input level at the rising edge of the clock.

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

T Flip-Flop

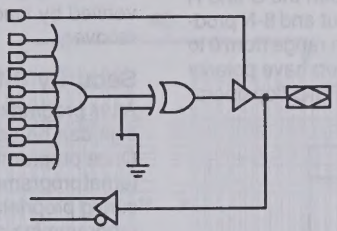
All 8 product terms are available to the OR gate. The T input polarity is controlled by an exclusive-OR gate. For the T register, the output level toggles when the T input is HIGH and remains the same when the T input is LOW.

T	Q^n	Q^{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

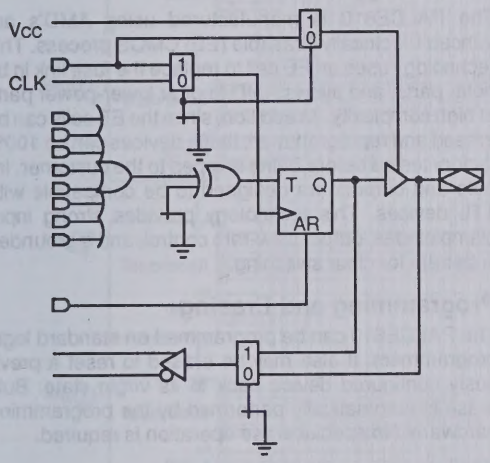
J–K Flip-Flop

The 8 product terms are divided between the J and K inputs. N product terms go to the J input and 8-N product terms go to the K input, where N can range from 0 to 8. Both the J and K inputs to the flip-flop have polarity control via exclusive-OR gates. The J–K flip-flop operation is shown below.

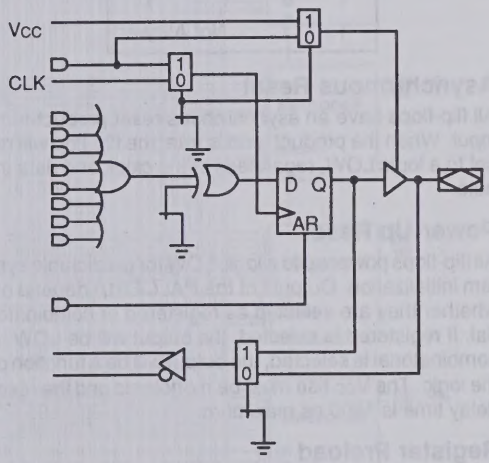
J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



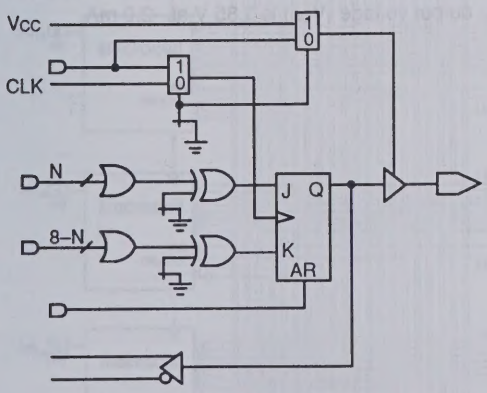
Combinatorial



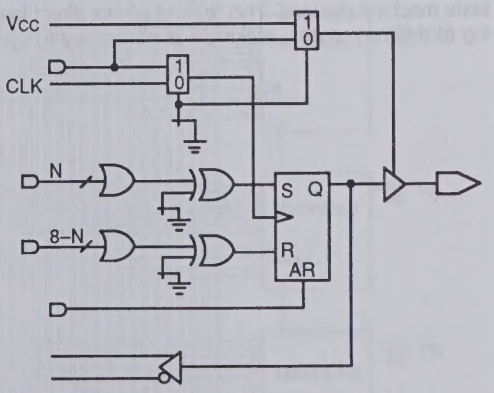
T Register



D Register



J–K Register



S–R Register

12950-004A

Figure 1. Macrocell Configurations

S–R Flip-Flop

The 8 product terms are divided between the S and R inputs. N product terms go to the S input and 8-N product terms go to the R input, where N can range from 0 to 8. Both the S and R inputs to the flip-flop have polarity control via exclusive-OR gates. The S–R flip-flop operation is shown below.

S	R	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Not Allowed	

Asynchronous Reset

All flip-flops have an asynchronous-reset product-term input. When the product term is true, the flip-flop will reset to a logic LOW, regardless of the clock and data inputs.

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE610 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW. If combinatorial is selected, the output will be a function of the logic. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE610 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE610 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during the erase cycle. Preload is not affected by the security bit.

Technology

The PALCE610 is manufactured using AMD's advanced Electrically Erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link in bipolar parts, and allows AMD to offer lower-power parts of high complexity. In addition, since the EE cells can be erased and reprogrammed, these devices can be 100% factory tested before being shipped to the customer. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clear switching.

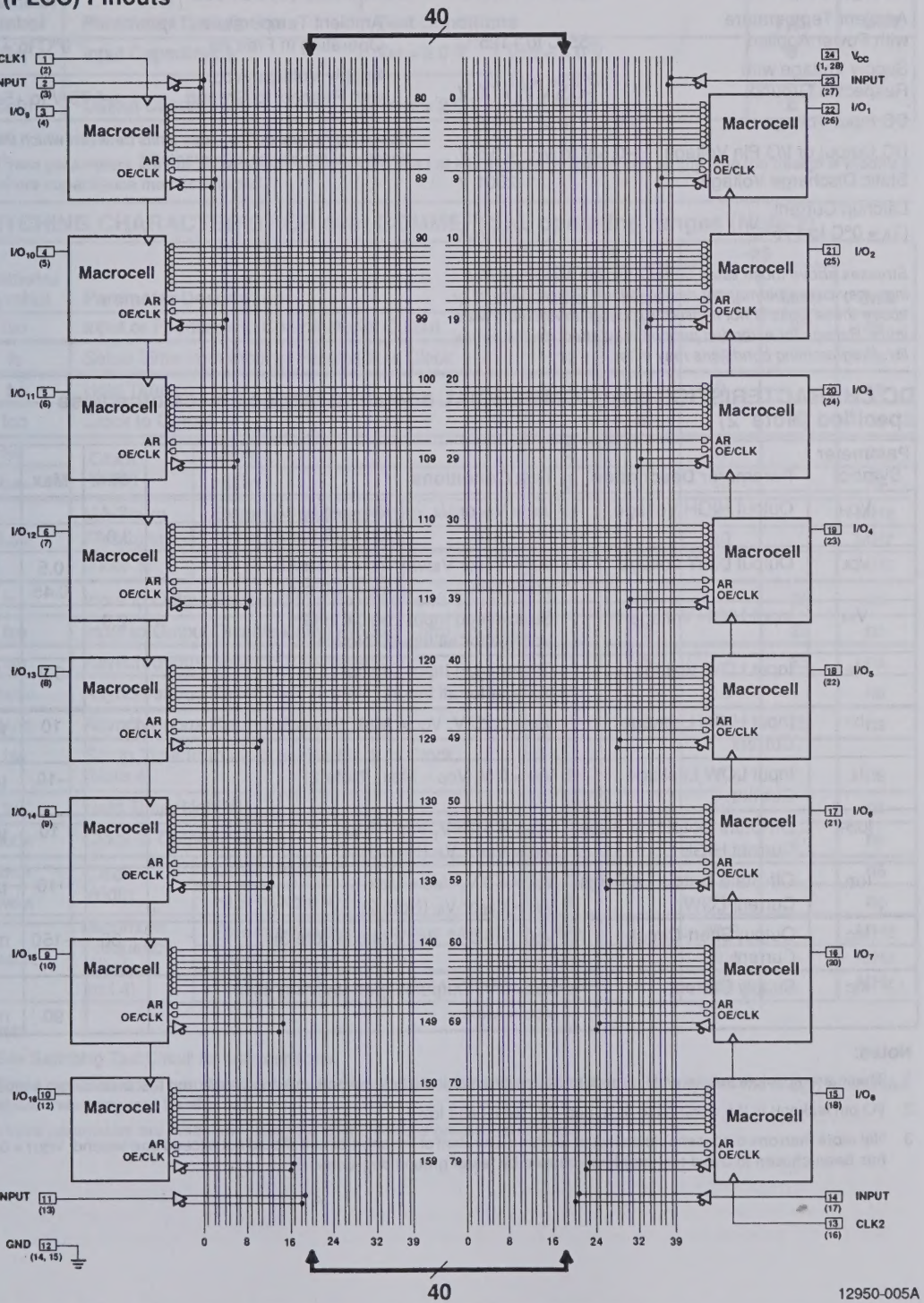
Programming and Erasing

The PALCE610 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Bulk erase is automatically performed by the programming hardware. No special erase operation is required.

CMOS Compatibility

The PALCE610 has CMOS-compatible outputs. The output voltage (V_{OH}) is 3.85 V at –2.0 mA.

PALCE610 LOGIC DIAGRAM
DIP (PLCC) Pinouts



12950-005A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	I_{OH} = –4.0 mA	2.4		V
			I_{OH} = –2.0 mA	3.84		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	I_{OL} = 8.0 mA		0.5	V
			I_{OL} = 4.0 mA		0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)		–30	–150	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.			90	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min.	-15 Max.	-25 Min.	-25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input or Feedback to Clock			12		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				8		12	ns
t_{WL}	Clock Width	LOW		6		10		ns
t_{WH}		HIGH		6		10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		37		MHz
		Internal Feedback (f_{CNT})		76.1		40		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	83.3		50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns
t_{AR}	Asynchronous Reset to Registered Output				15		25	ns
t_{ARW}	Asynchronous Reset Width			10		15		ns
t_{ARR}	Asynchronous Reset Recovery Time				15		25	ns
t_{SA}	Setup Time from Input or Feedback to Clock (Note 4)			5		8		ns
t_{HA}	Hold Time (Note 4)			5		12		ns
t_{COA}	Clock to Output (Note 4)				15		27	ns
t_{WLA}	Clock Width	LOW (Note 4)		6		10		ns
t_{WHA}		HIGH (Note 4)		6		10		ns
f_{MAXA}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_{SA} + t_{COA})$	50		28.6		MHz
		Internal Feedback (f_{CNT})		61.6		29.4		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$	83.3		50		MHz

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are measured using the asynchronous product-term clock.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are 100% tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	I_{OH} = –2 mA I_{OH} = –1 mA	2.4 3.84		V
V_{OL}	Output LOW Voltage	I_{OL} = 4 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5.0 V, T_A = 25° C (Note 5)		–30	–150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT}= 0 A) V_{CC} = Max.			90	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-833, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at anytime the design is modified where I_{OS} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	VCC T_A = +25°C f = 1 MHz	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

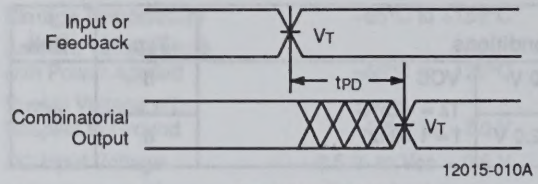
SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description			-20 Min.	-20 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output				20	ns
t_S	Setup Time from Input or Feedback to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	40		MHz
		Internal Feedback (f_{CNT})		50		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control (Note 3)				20	ns
t_{ER}	Input to Output Disable Using Product Term Control (Note 3)				20	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width (Note 3)			20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)				20	ns
t_{SA}	Setup Time from Input or Feedback to Clock (Note 4)			8		ns
t_{HA}	Hold Time (Note 4)			10		ns
t_{COA}	Clock to Output (Note 4)				20	ns
t_{WLA}	Clock Width	LOW (Note 4)		8		ns
t_{WHA}		HIGH (Note 4)		8		ns
f_{MAXA}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_{SA} + t_{COA})$	35.8		MHz
		Internal Feedback (f_{CNT})		45		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$	52.6		MHz

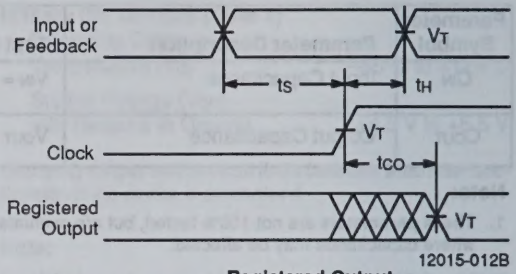
Notes:

2. See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
4. These parameters are measured using the asynchronous product-term clock.

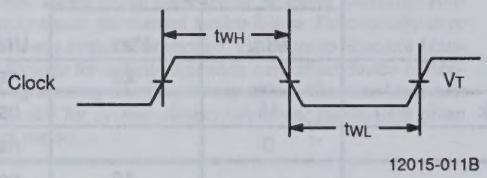
SWITCHING WAVEFORMS



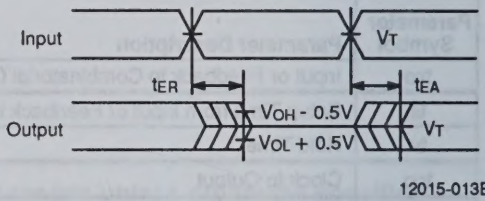
Combinatorial Output



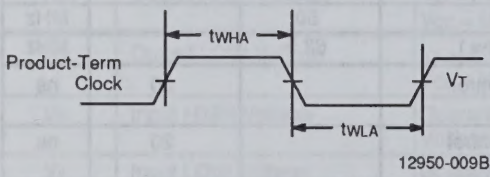
Registered Output



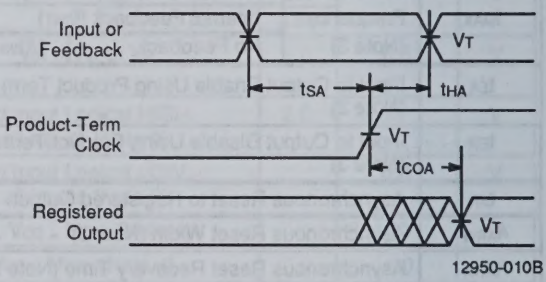
Clock Width



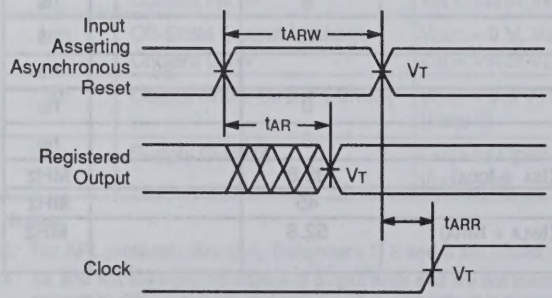
Input to Output Disable/Enable



Clock Width Using Product-Term Clock



Registered Output Using Product-Term Clock



Asynchronous Reset

Notes:

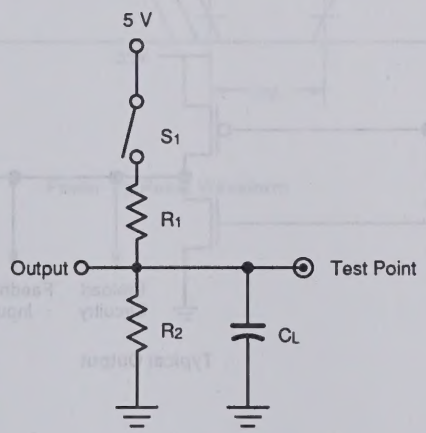
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



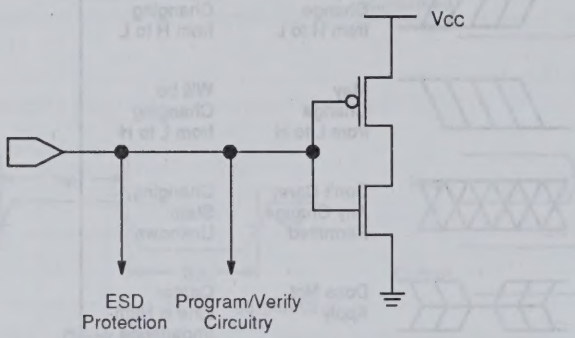
12950-012A

Specification	S_1	C_L	Commercial		Military		Measured Output Value
			R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF	855 Ω	340 Ω	855 Ω	340 Ω	1.5 V
t_{EA}	Z → H : Open Z → L : Closed	35 pF	855 Ω	340 Ω	855 Ω	340 Ω	1.5 V
t_{ER}	H → Z : Open L → Z : Closed	5 pF	855 Ω	340 Ω	855 Ω	340 Ω	H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

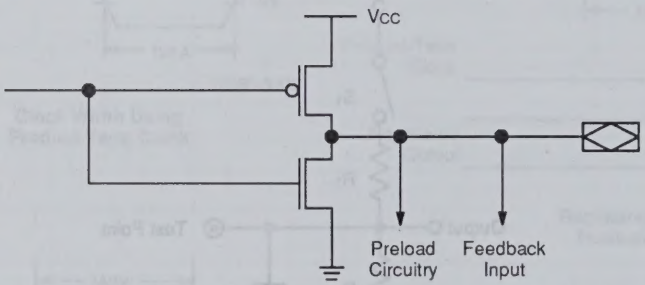
ENDURANCE

Symbol	Parameter Description	Test Conditions	Min.	Unit
t_{DR}	Pattern Data Retention Time	Max. Storage Temperature	10	Years
		Max. Operating Temperature	20	Years
N	Reprogramming Cycles	Normal Programming Conditions	100	Cycles

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Typical Input



Typical Output

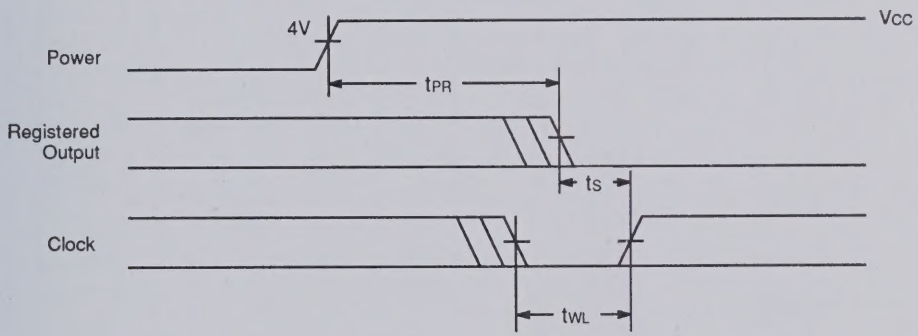
12950-011A

Power-Up Reset

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

PAL

CHAPTER 3
General Information

Military PAL Devices 3–3
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f_{MAX} Parameters 3–17
Physical Dimensions 3–18

PAL

Military PAL Devices

Advanced Micro Devices' Military Programmable Array Logic (PAL) devices provide state machine and combinatorial logic solutions processed to military criteria. We offer the largest number of Standard Military Drawing PAL products in the industry.

Applications for our configurable PAL architectures include counters, shift registers, accumulators, control sequence generators, decoders, multiplexers, adders, memory mapped I/O and much more. These designs go into radar systems, missile guidance, avionics, airport graphic terminals, parallel processors, military computer hardware, and product obsolescence solutions, just to name a few.

Military PAL Device Menu

Family	Part Number	Package	Technology	Inputs	I/O	Outputs	Product Terms/Output	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
16R8	PAL16L8-10	/BRA	TTL	10	6 Comb	2 Comb	7	10	10	210
	PAL16R8-10	/B2A		8	–	8 Reg	8			
	PAL16R6-10			8	2 Comb	6 Reg	7,8			
	PAL16R4-10			8	4 Comb	4 Reg	7,8			
	PAL16L8-12	/BRA						12	47.6	210
	PAL16R8-12	/B2A								
	PAL16R6-12									
	PAL16R4-12									
	PAL16L8B	20L, J, W						20	28.5	180
	PAL16R8B									
	PAL16R6B									
	PAL16R4B									
	PAL16L8B-2							30	20	90
	PAL16R8B-2									
	PAL16R6B-2									
	PAL16R4B-2									
	PAL16L8A							30	20	180
	PAL16R8A									
	PAL16R6A									
	PAL16R4A									
	PAL16L8B-4							50	13.3	55
	PAL16R8B-4									
	PAL16R6B-4									
	PAL16R4B-4									
20R8	PAL20L8-10	/BLA, /B3A	TTL	14	6 Comb	2 Comb	7	10	50	210
	PAL20R8-10			12	–	8 Reg	8			
	PAL20R6-10			12	2 Comb	6 Reg	7,8			
	PAL20R4-10			12	4 Comb	4 Reg	7,8			
	PAL20L8-12							12	41.7	210
	PAL20R8-12									
	PAL20R6-12									
	PAL20R4-12									
	PAL20L8-15							15	35.7	210
	PAL20R8-15									
	PAL20R6-15									
	PAL20R4-15									

Military PAL Device Menu (Continued)

Family	Part Number	Package	Technology	Inputs	I/O	Outputs	Product Terms/Output	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
20R8	PAL20L8B	24JS, W, 28L	TTL	14	6 Comb	2 Comb	7	20	28.5	210
	PAL20R8B			12	–	8 Reg	8			
	PAL20R6B			12	2 Comb	6 Reg	7,8			
	PAL20R4B			12	4 Comb	4 Reg	7,8			
	PAL20L8A							30	20	210
	PAL20R8A									
	PAL20R6A									
	PAL20R4A									

Universal PAL Devices

Family	Part Number	Package	Technology	Inputs	I/O	Product Terms/Output	Features	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
22V10	PAL22V10-12	/BLA, /BKA	TTL	12	10 Macro	8-16	Varied Term	12	50	200
	PAL22V10-20							20	31.2	200
	AmPAL22V10A	/B3A					Distribution	30	22	180
	AmPAL22V10							40	16.5	180
	PALCE22V10H-10		EE CMOS					10	62.5	150
	PALCE22V10H-15							15	50	120
	PALCE22V10H-20							20	33.3	120
	PALCE22V10H-25							25	26.3	100
	PALCE22V10H-30							30	25	100
20V8	PALCE20V8H-15	/BLA, /B3A	EE CMOS	12	8 Macro	8	GAL® Device Equivalent	15	41.6	130
	PALCE20V8H-20							20	33.3	130
	PALCE20V8H-25							25	25	130
16V8	PALCE16V8H-10	/BRA, /B2A	EE CMOS	8	8 Macro	8	GAL® Device Equivalent	10	58.5	130
	PALCE16V8H-15							15	41.6	130
	PALCE16V8H-20							20	33.3	130
	PALCE16V8H-25							25	28.6	130

Asynchronous PAL Device

Family	Part Number	Package	Technology	Inputs	Macro	Product Terms/Output	Clock Cells	Other Features	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
610	PALCE610H-20	/BLA, /B3A	EE CMOS	4	16	8	Program-mable	J-K Flip-Flops	20	35.8	90

MACH Family (Macro Array CMOS High-density)

Family	Part Number	Package	Technology	Inputs	Output Macro	Buried Macros	Product Terms/Output	t_{PD} ns	f_{MAX} MHz	I_{CC} mA
MACH 1	MACH110–20	44CQFP	EE CMOS	6	32	–	0–12	20	40	170
MACH 1	MACH130–20	84CQFP	EE CMOS	6	64	–	0–12	20	40	220
MACH 2	MACH210–20	44CQFP	EE CMOS	6	32	32	0–16	20	40	195
MACH 2	MACH230–20	84CQFP	EE CMOS	6	64	32	0–16	20	40	–

Standard Military Drawing Program

AMD is an active participant in the Standard Military Drawing (SMD) Program. The idea behind the SMD Program is to standardize MIL-STD-883, Class B microcircuits. The advantage to the user is that SMDs are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.

Standard Military Drawings should always be considered to improve availability over source control drawings. It is standard practice at AMD to convert our 883, Class B processing to SMDs for all products which we are approved to supply. AMD then dual marks these devices with both the SMD number and the Generic Part Number. DESC approved products can then be procured to either part number as standard product through both OEM and Distributor channels.

AMD will continue to work closely with DESC, generating new drawings, which will provide a steady flow of advanced technology products to standardize specifications.

Product Introduction Procedures

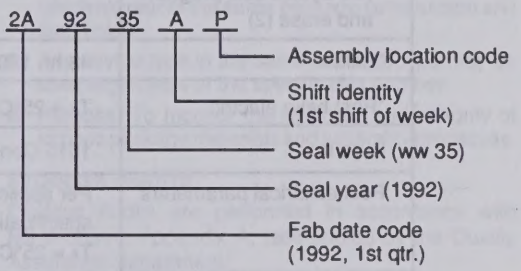
All new military products released by the Programmable Logic Products Division must successfully pass MIL-STD-883 Class B processing prior to new product announcement. This practice allows us to do checkout of bonding diagrams, electrical test tapes and burn circuits in a manufacturing environment. Programmability is checked when applicable. Our Engineering Department reviews electrical data to insure performance and yields to military data sheet limits are acceptable, prior to new product release. This procedure allows AMD to keep manufacturing start-up problems to a minimum on new product orders.

Manufacturing and Screening Locations

MIL-STD-883 Class B products, and orders to source control drawings, are assembled at our Penang, Malaysia facility. This facility is qualified by AMD Quality Department, as well as by many of our customers, to manufacture non-MIL-STD-883 Class B products. Conformance to MIL-STD-883 requirements is routinely monitored through audits at the Penang facility.

Assembly location as well as fabrication and seal date codes are included in AMD's part marking.

Example:



Assembly Location Codes:

Blank	Sunnyvale
M	Manila
P	Penang

Standard Military Flow Chart

Screening	Class B	Requirements
Assembly	Offshore assembly	
Internal visual	2010 cond. B	100%
Temperature cycling	1010	100%
Constant acceleration	2001 test cond. D or E Y1 orientation only	100%
Interim electrical parameter (1)	Per applicable device (1) specification T_A = 25°C only	100%
*100 Cycles bulk program and erase (2)		100%
*Bake	48 hr. 150°C	100%
*Post bake electric	T_A = 25°C	100%
Burn In	1015 Cond. C or D	100%
Post electrical parameters	Per applicable device specification T_A = 25°C only	100%
Percent defect allowable	DC Parameters PDA = 5% or 1 device whichever is greater	
Final electrical parameters (hot and cold extremes)	Per applicable device specification	100%
Seal A) Fine B) Gross	1014 Cond, A or B cond C	100%
Group A lot	5005 Class B	Sample every lot
Group B inspection lot Group C Group D External visual	5005 Class B 5005 Class B 5005 Class B 2009	Every lot Every 4 qtrs. of fab date code Every 52 weeks 100%

*EE CMOS Devices

(1) Programming and verification are performed at 25°C only

(2) May be performed at wafer sort.

Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

Mil-M-38510, Appendix A, "Product Assurance Program"

Mil-0-9858, "Quality Program Requirements"

Mil-1-45208, "Inspection System Requirements"

Quality Assurance

The Programmable Logic Products Division ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of MIL-STD-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

For products requiring programming prior to AC tests, testing is performed utilizing MIL-M-38510 slash sheet sample plans and approved SMD sample plans.

Product Qualification/Quality Conformance Inspection (QCI)

AMD has a quality conformance testing program in accordance with MIL-STD-883, Method 5005. Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that AMD, as a minimum, conduct qualification testing per Company Policy specification on Product Reliability Qualification (00–021). Once qualified, each package type (from each assembly line) and device (by technology group as delineated in MIL-M-38510) are incorporated into AMD Quality Conformance Inspection program which utilizes the requirements of MIL-STD-883.

When military programs do not require that QCI data be run on the specific lot shipped, AMD Quality Conformance program allows customers to obtain generic data on all product families manufactured by AMD Generic Qualification Data enables customers to eliminate costly qualification and destruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following product data is available:

Group B – Package Related Tests

- QCI is performed in line on each inspection lot.
- Purpose: To monitor assembly and device package integrity.

Group C – Product/Process Related Tests

- Group C is performed based on fab date code, at least every four quarters.
- Life test data may be used to qualify similar technologies.
- Purpose: To monitor the reliability of the process and the parametric performance for each product technology.

Group D – In-Depth Package Related Tests

- QCI is conducted every 52 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.

Process Audits

Process Audits are performed in accordance with Mil-M-38510, Appendix A, (self audits) by the Quality Assurance Department.

Electrostatic Discharge Control Procedures

AMD fully employs static control procedures throughout its facilities.

All manufacturing areas where product is processed or handled including our Reliability Labs, Engineering Labs, etc., have full static control such as wrist straps, antistatic smocks, grounded stainless steel tables, conductive mats and ion generators wherever necessary.

All product is moved throughout our facilities and shipped to customers in static shielded containers.

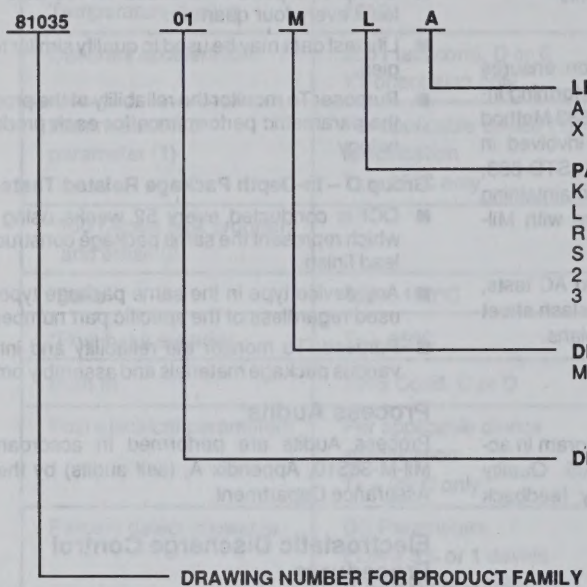
In addition, AMD distributors must demonstrate that they meet the same stringent standards regarding ESD handling and control procedures as the factory. Individual distributor locations are audited and approved annually by AMD's Quality Assurance Department.

An ESD identifier is marked on all products per MIL-STD-883 1.2.1 b (30). All shipping containers are labeled with an ESD Caution Message. ESD procedures are continually reviewed, to ensure that our customers receive only the highest quality product from AMD.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:



PART NUMBER INTERPRETATION:
When ordering to Military Drawing numbers, the lead finish designator (last letter in part number) is commonly called out as "X". This is a way of stating that the customer will accept the standard manufacturer's lead finish for the package orders. "X" is not a lead finish designator in itself, therefore, when product is shipped, the actual lead finish designator will be marked on the devices.

Military SMDs

Military Drawing	AMD Part Number	Military Drawing	AMD Part Number
8103501RA	PAL10H8MJ/883B	84129033A	PAL20R6AML/883B
81035012A	PAL10H8ML/883B	8412903KA	PAL20R6AMW/883B
8103501SA	PAL10H8MW/883B	8412904LA	PAL20R4AMJS/883B
8103502RA	PAL12H6MJ/883B	84129043A	PAL20R4AML/883B
81035022A	PAL12H6ML/883B	8412904KA	PAL20R4AMW/883B
8103502SA	PAL12H6MW/883B	8412905LA	PAL20L10AMJS/883B
8103503RA	PAL14H4MJ/883B	84129053A	PAL20L10AML/883B
81035032A	PAL14H4ML/883B	8412905KA	PAL20L10AMW/883B
8103503SA	PAL14H4MW/883B	8412906LA	PAL20X8AMJS/883B
8103504RA	PAL16H2MJ/883B	84129063A	PAL20X8AML/883B
81035042A	PAL16H2ML/883B	8412906KA	PAL20X8AMW/883B
8103504SA	PAL16H2MW/883B	8412907LA	PAL20X10AMJS/883B
8103505RA	PAL16C1MJ/883B	84129073A	PAL20X10AML/883B
81035052A	PAL16C1ML/883B	8412907KA	PAL20X10AMW/883B
8103505SA	PAL16C1MW/883B	8412908LA	PAL20X4AMJS/883B
8103506RA	PAL10L8MJ/883B	84129083A	PAL20X4AML/883B
81035062A	PAL10L8ML/883B	8412908KA	PAL20X4AMW/883B
8103506SA	PAL10L8MW/883B	8412909LA	PAL20L8A-2MJS/883B
8103507RA	PAL12L6MJ/883B	84129093A	PAL20L8A-2ML/883B
81035072A	PAL12L6ML/883B	8412909KA	PAL20L8A-2MW/883B
8103507SA	PAL12L6MW/883B	8412910LA	PAL20R8A-2MJS/883B
8103508RA	PAL14L4MJ/883B	84129103A	PAL20R8A-2ML/883B
81035082A	PAL14L4ML/883B	8412910KA	PAL20R8A-2MW/883B
8103508SA	PAL14L4MW/883B	8412911LA	PAL20R6A-2MJS/883B
8103509RA	PAL16L2MJ/883B	84129113A	PAL20R6A-2ML/883B
81035092A	PAL16L2ML/883B	8412911KA	PAL20R6A-2MW/883B
8103509SA	PAL16L2MW/883B	8412912LA	PAL20R4A-2MJS/883B
8103607RA	PAL16L8AMJ/883B	84129123A	PAL20R4A-2ML/883B
81036072A	PAL16L8AML/883B	8412912KA	PAL20R4A-2MW/883B
8103607SA	PAL16L8AMW/883B	8506501RA	PAL16L8A-4MJ/883B
8103608RA	PAL16R8AMJ/883B	85065012A	PAL16L8A-4ML/883B
81036082A	PAL16R8AML/883B	8506501SA	PAL16L8A-4MW/883B
8103608SA	PAL16R8AMW/883B	8506502RA	PAL16R8A-4MJ/883B
8103609RA	PAL16R6AMJ/883B	85065022A	PAL16R8A-4ML/883B
81036092A	PAL16R6AML/883B	8506502SA	PAL16R8A-4MW/883B
8103609SA	PAL16R6AMW/883B	8506503RA	PAL16R6A-4MJ/883B
8103610RA	PAL16R4AMJ/883B	85065032A	PAL16R6A-4ML/883B
81036102A	PAL16R4AML/883B	8506503SA	PAL16R6A-4MW/883B
8103610SA	PAL16R4AMW/883B	8506504RA	PAL16R4A-4MJ/883B
8103612RA	PAL16R8A-2MJ/883B	85065042A	PAL16R4A-4ML/883B
81036122A	PAL16R8A-2ML/883B	8506504SA	PAL16R4A-4MW/883B
8103612SA	PAL16R8A-2MW/883B	5962-8515501RA	PAL16L8BMJ/883B
8103613RA	PAL16R6A-2MJ/883B	5962-85155012A	PAL16L8BML/883B
81036132A	PAL16R6A-2ML/883B	5962-8515501SA	PAL16L8BMW/883B
8103613SA	PAL16R6A-2MW/883B	5962-8515502RA	PAL16R8BMJ/883B
8103614RA	PAL16R4A-2MJ/883B	5962-85155022A	PAL16R8BML/883B
81036142A	PAL16R4A-2ML/883B	5962-8515502SA	PAL16R8BMW/883B
8103614SA	PAL16R4A-2MW/883B	5962-8515503RA	PAL16R6BMJ/883B
8412901LA	PAL20L8AMJS/883B	5962-85155032A	PAL16R6BML/883B
84129013A	PAL20L8AML/883B	5962-8515503SA	PAL16R6BMW/883B
8412901KA	PAL20L8AMW/883B	5962-8515504RA	PAL16R4BMJ/883B
8412902LA	PAL20R8AMJS/883B	5962-85155042A	PAL16R4BML/883B
84129023A	PAL20R8AML/883B	5962-8515504SA	PAL16R4BMW/883B
8412902KA	PAL20R8AMW/883B	5962-8515505RA	PAL16L8B-2MJ/883B
8412903LA	PAL20R6AMJS/883B	5962-85155052A	PAL16L8B-2ML/883B

Military SMDs (Continued)

Military Drawing	AMD Part Number	Military Drawing	AMD Part Number
5962-8515505SA	PAL16L8B-2MW/883B	5962-8680401KA	PAL18L4MW/883
5962-8515506RA	PAL16R8B-2MJ/883B	5962-8680402LA	PAL12L10MJS/883B
5962-85155062A	PAL16R8B-2ML/883B	5962-86804023A	PAL12L10ML/883B
5962-8515506SA	PAL16R8B-2MW/883B	5962-8680402KA	PAL12L10MW/883B
5962-8515507RA	PAL16R6B-2MJ/883B	5962-8680403LA	PAL14L8MJS/883B
5962-85155072A	PAL16R6B-2ML/883B	5962-86804033A	PAL14L8ML/883B
5962-8515507SA	PAL16R6B-2MW/883B	5962-8680403KA	PAL14L8MW/883B
5962-8515508RA	PAL16R4B-2MJ/883B	5962-8680404LA	PAL16L6MJS/883B
5962-85155082A	PAL16R4B-2ML/883B	5962-86804043A	PAL16L6ML/883B
5962-8515508SA	PAL16R4B-2MW/883B	5962-8680404KA	PAL16L6MW/883B
5962-8515509RA	PAL16L8DMJ/883B	5962-8680405LA	PAL20L2MJS/883B
5962-85155092A	PAL16L8DML/883B	5962-86804053A	PAL20L2ML/883B
5962-8515509SA	PAL16L8DMW/883B	5962-8680405KA	PAL20L2MW/883B
5962-8515510RA	PAL16R8DMJ/883B	5962-8680406LA	PAL20C1MJS/883B
5962-85155102A	PAL16R8DML/883B	5962-86804063A	PAL20C1ML/883B
5962-8515510SA	PAL16R8DMW/883B	5962-8680406KA	PAL20C1MW/883B
5962-8515511RA	PAL16R6DMJ/883B	5962-8753001LA	PAL20S10MJS/883B
5962-85155112A	PAL16R6DML/883B	5962-87530013A	PAL20S10ML/883B
5962-8515511SA	PAL16R6DMW/883B	5962-8753001KA	PAL20S10MW/883B
5962-8515512RA	PAL16R4DMJ/883B	5962-8753002LA	PAL20RS10MJS/883B
5962-85155122A	PAL16R4DML/883B	5962-87530023A	PAL20RS10ML/883B
5962-8515512SA	PAL16R4DMW/883B	5962-8753002KA	PAL20RS10MW/883B
5962-85155132A	PAL16L8-12/B2A	5962-8753003LA	PAL20RS8MJS/883B
5962-8515513RA	PAL16L8-12/BRA	5962-87530033A	PAL20RS8ML/883B
5962-85155142A	PAL16R8-12/B2A	5962-8753003KA	PAL20RS8MW/883B
5962-8515514RA	PAL16R8-12/BRA	5962-8753004LA	PAL20RS4MJS/883B
5962-85155152A	PAL16R6-12/B2A	5962-87530043A	PAL20RS4ML/883B
5962-8515515RA	PAL16R6-12/BRA	5962-8753004KA	PAL20RS4MW/883B
5962-85155162A	PAL16R4-12/B2A	5962-8767101LA	PAL20L8BMJS/883B
5962-8515516RA	PAL16R4-12/BRA	5962-87671013A	PAL20L8BML/883B
5962-85155172A	PAL16L8-10/B2A	5962-8767101KA	PAL20L8BMW/883B
5962-8515517RA	PAL16L8-10/BRA	5962-8767102LA	PAL20R8BMJS/883B
5962-85155182A	PAL16R8-10/B2A	5962-87671023A	PAL20R8BML/883B
5962-8515518RA	PAL16R8-10/BRA	5962-8767102KA	PAL20R8BMW/883B
5962-85155192A	PAL16R6-10/B2A	5962-8767103LA	PAL20R6BMJS/883B
5962-8515519RA	PAL16R6-10/BRA	5962-87671033A	PAL20R6BML/883B
5962-85155202A	PAL16R4-10/B2A	5962-8767103KA	PAL20R6BW/883B
5962-8515520RA	PAL16R4-10/BRA	5962-8767104LA	PAL20R4BMJS/883B
5962-8605301LA	AmPAL22V10A/BLA	5962-87671043A	PAL20R4BML/883B
5962-86053013A	AmPAL22V10A/B3A	5962-8767104KA	PAL20R4BMW/883B
5962-8605301KA	AmPAL22V10A/BKA	5962-8767107LA	PAL20L8-15/BLA
5962-8605302LA	AmPAL22V10/BLA	5962-87671073A	PAL20L8-15/B3A
5962-86053023A	AmPAL22V10/B3A	5962-8767108LA	PAL20R8-15/BLA
5962-8605302KA	AmPAL22V10/BKA	5962-87671083A	PAL20R8-15/B3A
5962-8605304LA	PAL22V10-20/BLA	5962-8767109LA	PAL20R6-15/BLA
5962-86053043A	PAL22V10-20/B3A	5962-87671093A	PAL20R6-15/B3A
5962-8605304KA	PAL22V10-20/BKA	5962-8767110LA	PAL20R4-15/BLA
5962-88063053A	PAL22V10-12/B3A	5962-87671103A	PAL20R4-15/B3A
5962-8605305KA	PAL22V10-12/BKA	5962-8767111LA	PAL20L8-12/BLA
5962-8605305LA	PAL22V10-12/BLA	5962-87671113A	PAL20L8-12/B3A
5962-8680301LA	PAL20RA10MJS/883B	5962-8767112LA	PAL20R8-12/BLA
5962-86803013A	PAL20RA10ML/883B	5962-87671123A	PAL20R8-12/B3A
5962-8680301KA	PAL20RA10MW/883B	5962-8767113LA	PAL20R6-12/BLA
5962-8680401LA	PAL18L4MJS/883B	5962-87671133A	PAL20R6-12/B3A
5962-86804013A	PAL18L4ML/883B	5962-8767114LA	PAL20R4-12/BLA

Military SMDs (Continued)

Military Drawing	AMD Part Number	Military Drawing	AMD Part Number
5962-87671143A	PAL20R4-12/B3A	5962-8983902RA	PALCE16V8H-20E4/BRA
5962-8767115LA	PAL20L8-10/BLA	5962-89839032A	PALCE16V8H-15E4/B2A
5962-87671153A	PAL20L8-10/B3A	5962-8983903RA	PALCE16V8H-15E4/BRA
5962-8767116LA	PAL20R8-10/BLA	5962-89840013A	PALCE20V8H-25E4/B3A
5962-87671163A	PAL20R8-10/B3A	5962-8984001LA	PALCE20V8H-25E4/BLA
5962-8767117LA	PAL20R6-10/BLA	5962-89840023A	PALCE20V8H-20E4/B3A
5962-87671173A	PAL20R6-10/B3A	5962-8984002LA	PALCE20V8H-20E4/BLA
5962-8767118LA	PAL20R4-10/BLA	5962-89840033A	PALCE20V8H-15E4/B3A
5962-87671183A	PAL20R4-10/B3A	5962-8984003LA	PALCE20V8H-15E4/BLA
5962-8851501RA	PAL16L8B-4MJ/883B	5962-89841013A	PALCE22V10H-30/B3A
5962-88515012A	PAL16L8B-4ML/883B	5962-8984101KA	PALCE22V10H-30/BKA
5962-8851501SA	PAL16L8B-4MW/883B	5962-8984101LA	PALCE22V10H-30/BLA
5962-8851502RA	PAL16R8-4MJ/883B	5962-89841023A	PALCE22V10H-20E4/B3A
5962-88515022A	PAL16R8B-4ML/883B	5962-8984102KA	PALCE22V10H-20E4/BKA
5962-8851502SA	PAL16R8B-4MW/883B	5962-8984102LA	PALCE22V10H-20E4/BLA
5962-8851503RA	PAL16R6B-4MJ/883B	5962-89841043A	PALCE22V10H-25/B3A
5962-88515032A	PAL16R6B-4ML/883B	5962-8984104KA	PALCE22V10H-25/BKA
5962-8851503SA	PAL16R6B-4MW/883B	5962-8984104LA	PALCE22V10H-25/BLA
5962-8851504RA	PAL16R4B-4MJ/883B	5962-89841053A	PALCE22V10H-15E4/B3A
5962-88515042A	PAL16R4B-4ML/883B	5962-8984105KA	PALCE22V10H-15E4/BKA
5962-8851504SA	PAL16R4B-4MW/883B	5962-8984105LA	PALCE22V10H-15E4/BLA
5962-89839012A	PALCE16V8H-25E4/B2A	5962-9169501M3A	PALCE610H-20/B3A
5962-8983901RA	PALCE16V8H-25E4/BRA	5962-9169501MLA	PALCE610H-20/BLA
5962-89839022A	PALCE16V8H-20E4/B2A		

The Advantages

An important service that AMD's Programmable Logic Division offers is ProPAL devices, the programming of a customer's PAL devices during the manufacturing cycle, saving aerospace customers significant time and money. We offer full 883, SMD, programmed products. Not only were we the first to offer this service, we by far have the most expertise in managing your programmed business.

The pre-programming of PAL devices for the customer offers a number of advantages, most of which increase the parts' reliability. Unlike a blank generic device, a ProPAL device undergoes a more thorough testing process. Listed below are just a few of the many advantages.

Enhanced Reliability

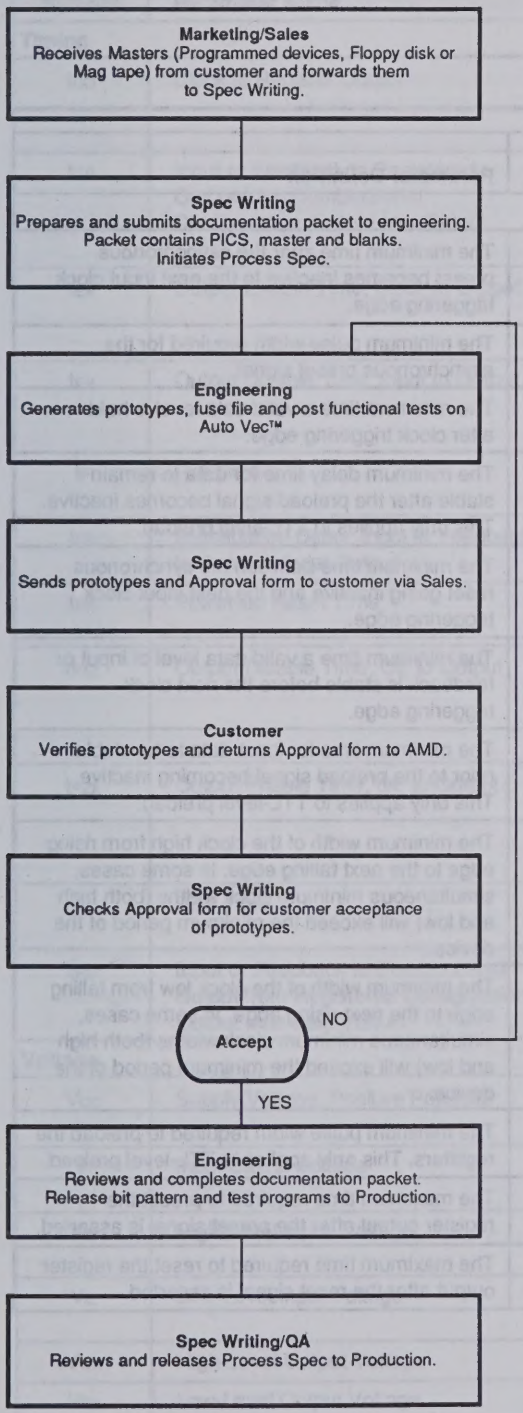
- In the design environment, the pattern undergoes fault simulation with > 90% coverage, providing a high testability. (Some patterns do not allow 90% fault coverage. In those cases the customer will be notified.)
- The parts are programmed prior to burn-in; weak parts are likely to fail to accept a program and be rejected on the spot.
- Programmed devices then must pass 25°C DC, functional and AC electrical tests prior to burn-in and DC, functional and AC electrical tests after burn-in, at temperature extremes, per M5004.

Although the price of the ProPAL device is higher than that of its unprogrammed counterpart, the added value provided to the user more than offsets the cost. In this era of cost-cutting and the need to get the most from each dollar spent, ProPAL devices make it possible for the customer to save money over the life of the project. Below are just a few examples of where cost savings can be recognized.

Cost Reduction Areas:

- The more thorough testing significantly increases the long term reliability of the device. System failures and resulting rework costs, owing to a defective PAL device, can easily be 50 times the purchase price of the component.
- The customer does not have to purchase and maintain costly programming and test facilities. He can concentrate on what he does best. . .design systems to aid in defense of our nation and allow AMD to do what we do best. . .produce and test Programmable Logic Devices.
- As volumes go up, the customer's production line won't be constrained by his programming and labeling capacities or throughput time.
- Inventories can be reduced. The customer no longer needs to store extra product for programming fall-out or human error.
- Improve lead time of manufacturing. The customer will no longer need to plan on internal time to program or label devices.

ProPAL Device Flow for Products with Existing Mil Shell Programs



Military Programming Process Summary

(per current Revisions of Mil–Std-883 and Mil-M-38510)

Assembly

Initial Electrical Test (25°C)	– 100% program to customer bit pattern
	– 100% DC/Functional/AC at 25°C, M5004
Burn-In	– Method 1015, Condition C or D
Electrical Test (25°C)	– 100% DC/Functional/AC at 25°C per M5004
	– Group A DC/Functional/ AC at 25°C per M5005
PDA	– 5% (DC only)
Solder Dip	
Mark	
Lot B Test	– Resistance to solvents, solderability, bond pull
	– M5005
Electrical Test (+125°C &–55°C)	– 100% DC/Functional/ AC, M5004
	– Group A DC/Functional/ AC, M5005
Hermiticity	– 100% Fine/Gross Leak per Method 1014
External Visual	– Method 2009
Data Review/Pack/Ship	

AMD is the proven technology leader in PAL devices and has numerous years of experience in programming customer patterns. Currently several major customers are using ProPAL devices and several major programs are being converted to ProPAL devices. Factory programming of your PAL device products is another service of the Military Programmable Logic's long-term partnership with and commitment to the worldwide Military and Aerospace market. For more information on Military ProPAL devices contact your local AMD sales office.

Electrical Characteristic Definitions

Parameter Symbol	Parameter Name	Parameter Definition
Timing		
t_{APR}	Asynchronous Preset Recovery Time	The minimum time after the asynchronous preset becomes inactive to the next input clock triggering edge.
t_{APW}	Asynchronous Preset Width	The minimum pulse width required for the asynchronous preset signal.
t_H	Hold Time	The minimum time a valid data level is held after clock triggering edge.
t_{HP}	Hold Time for Preload	The minimum delay time for data to remain stable after the preload signal becomes inactive. This only applies to TTL-level preload.
t_{SRR}	Synchronous Reset Recovery Time	The minimum time between the synchronous reset going inactive and the next input clock triggering edge.
t_S	Setup Time, Input or Feedback to Clock	The minimum time a valid data level of input or feedback is stable before the next clock triggering edge.
t_{SP}	Data Setup Time for Preload	The minimum time for input data to be stable prior to the preload signal becoming inactive. This only applies to TTL-level preload.
t_{WH}	Clock Width High	The minimum width of the clock high from rising edge to the next falling edge. In some cases, simultaneous minimum clock widths (both high and low) will exceed the minimum period of the device.
t_{WL}	Clock Width Low	The minimum width of the clock low from falling edge to the next rising edge. In some cases, simultaneous minimum clock widths (both high and low) will exceed the minimum period of the device.
t_{WP}	Preload Pulse Width	The minimum pulse width required to preload the registers. This only applies to TTL-level preload.
t_{AP}	Asynchronous Preset to Output	The maximum time required to preset the register output after the preset signal is asserted.
t_{AR}	Asynchronous Reset to Output	The maximum time required to reset the register output after the reset signal is asserted.

Parameter Symbol	Parameter Name	Parameter Definition
Timing		
t_{CO}	Clock to Register Output	The maximum time it takes to obtain a valid data level on the output pin after an input clock triggering edge is applied.
t_{CR}	Input or Feedback to Registered Output from Combinatorial Configuration; Output Mux Select 1 to 0	The minimum time from input or feedback to registered output as output mux selection changes from combinatorial to registered output 1 to 0).
t_{EA}	Output Enable Time, Clock to Output	The minimum delay between when an input is asserted and the output switches from a high-impedance state to HIGH or LOW logic state.
t_{ER}	Output Disable Time, Input to Output	The minimum delay between when an input is asserted and the output switches from a HIGH or LOW logic state to a high-impedance state.
t_F	Fall Time	The minimum time for a signal to fall from 80% to 20% of its stabilized high value.
t_{PD}	Propagation Delay, Input or Feedback to Combinatorial Output	The time for a signal to propagate from input or feedback to output.
t_{PR}	Power-up Reset Time	The minimum time for a registered output signal to be reset after the power is applied.
t_{PXZ}	Output Disable Time, OE to Output	The minimum delay between when a dedicated enable signal is asserted and the output switches from a HIGH or LOW logic state to be a high-impedance state.
t_{PZX}	Output Enable Time, OE to Output	The minimum delay between when a dedicated enable signal is asserted and the output switches from a high-impedance state to a HIGH or LOW logic state.
t_R	Rise Time	The minimum time for a signal to rise from 20% to 80% of its stabilized high value.
t_{RC}	Input or Feedback to Combinatorial Output from Registered Configuration; Output Mux Select 0 to 1	The minimum time from input or feedback to combinatorial output mux selection changes from registered to combinatorial output (0 to 1).
Voltage		
V_{CC}	Supply Voltage, Positive Potential	The voltage required across supply and ground terminals of a TTL or CMOS integrated circuit.
V_I	Input Clamp Voltage	The maximum input clamp voltage limit on every input pin.
V_{IH}	High-Level Input Voltage	The minimum high-level input voltage that is guaranteed to represent a high logic level.
V_{IL}	Low-Level Input Voltage	The maximum low-level input voltage that is guaranteed to represent a low logic level.
V_{OH}	High-Level Output Voltage	The minimum high logic level guaranteed for all outputs.
V_{OL}	Low-Level Output Voltage	The minimum low logic level guaranteed for all outputs.

Parameter Symbol	Parameter Name	Parameter Definition
Current		
I_{CC}	Supply Current, Corresponding to V_{CC}	The maximum current into the V_{CC} terminal of a TTL or CMOS integrated circuit.
I_I	Input Current with Maximum Input Voltage	The maximum current into an input pin when the input voltage is applied to the input pin.
I_{IH}	High-Level Input Current	The maximum current into an input pin when a logic-high level is applied to the input pin.
I_{IL}	Low-Level Input Current	The maximum current into an input pin when a logic-low level is applied to the input pin.
I_{OH}	High-Level Output Current	The maximum current into an output pin to guarantee an output logic-high level.
I_{OL}	Low-Level Output Current	The maximum current into an output pin to guarantee an output logic-low level.
I_{SC}	Output Short-Circuit Current	The current into an output when that output is short-circuited to ground (0.5 V).
I_{OZH}	High-Level Leakage Current	The maximum current into a high-impedance state output pin when a high logic level is applied to the output pin.
I_{OZL}	Low-Level Leakage Current	The maximum current into a high-impedance state output pin when a low logic level is applied to the output pin.
Miscellaneous		
C_{IN}	Input Capacitance	The input pin capacitance at a specified voltage and frequency.
C_{OUT}	Output Capacitance	The output or I/O pin capacitance at a specified voltage and frequency.
T_A	Operating Free Air Temperature	The ambient homogeneous temperature of the environment during operation.
T_C	Operating Case Temperature	The maximum chassis temperature during operation.
f_{MAX}	Maximum External Frequency	The $f_{MAX,\ External}$ is the maximum clocking frequency with external feedback. It is the reciprocal of the clock period ($t_s + t_{CO}$).
f_{MAX}	Maximum Internal Frequency	The $f_{MAX,\ Internal}$ is the maximum clocking frequency with internal feedback. An internal counter is used to determine "f_{CNT}."
f_{MAX}	Maximum Frequency without Feedback	The $f_{MAX,\ No\ Feedback}$ is the maximum clocking frequency with no feedback. It is the reciprocal of the sum of the data setup time (t_s) and the data hold time (t_h).

f_{MAX} Parameters

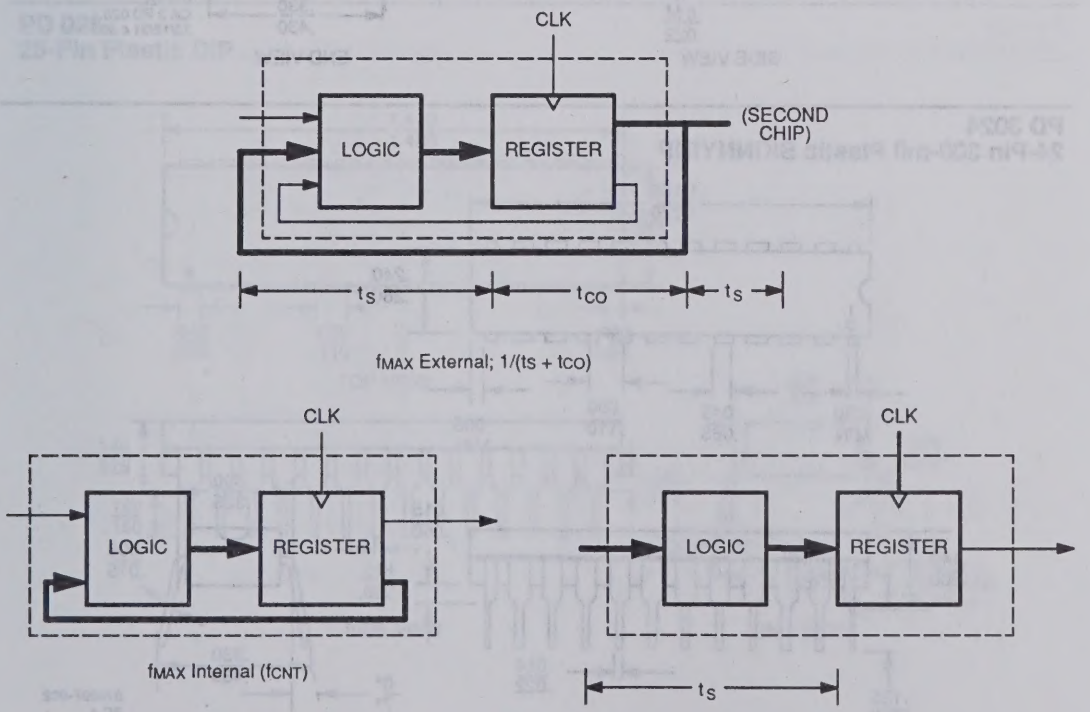
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external".

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design, therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback".

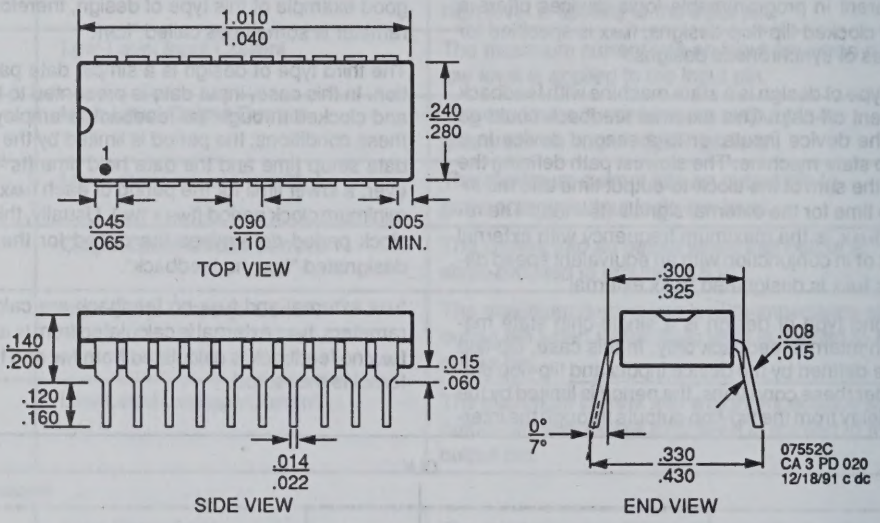
f_{MAX} external and f_{MAX} no feedback are calculated parameters. f_{MAX} external is calculated from t_S and t_{CO}, and f_{MAX} no feedback is calculated from t_{WL} and t_{WH}. f_{MAX} internal is measured.



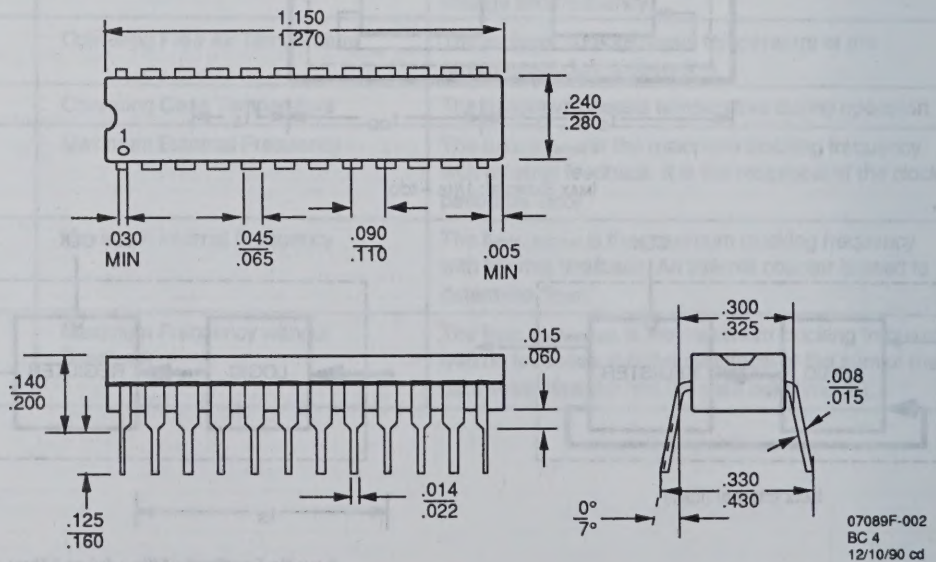
12222C-007B

Physical Dimensions*

PD 020
20-Pin Plastic DIP

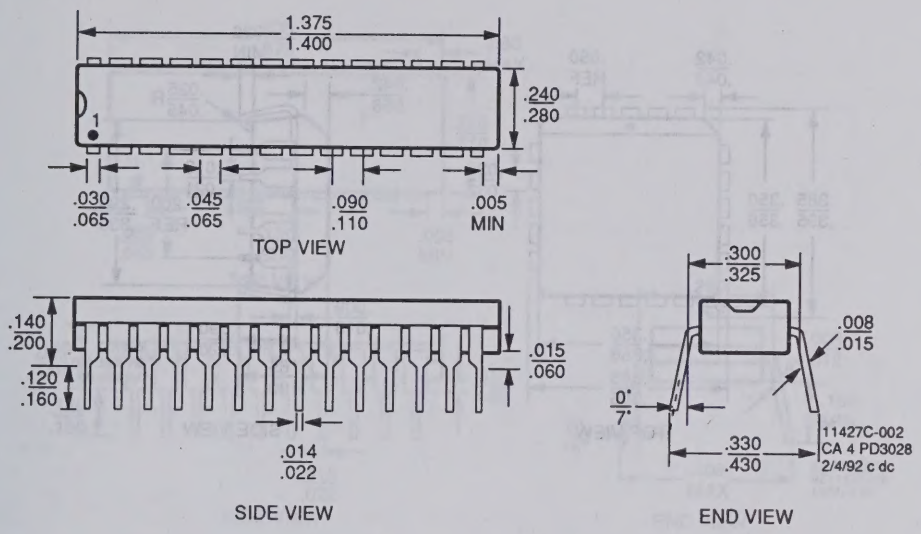


PD 3024
24-Pin 300-mil Plastic SKINNYDIP

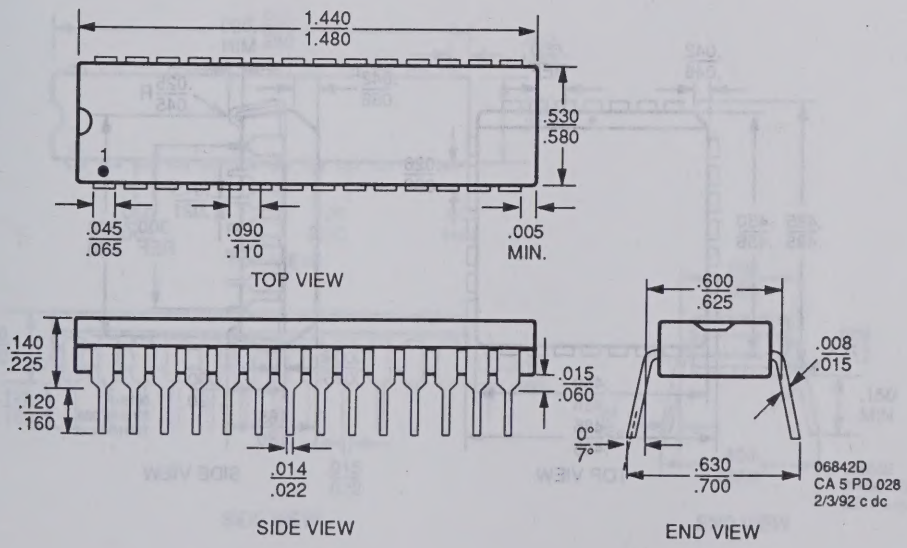


*For reference only. All dimensions measured in inches. BSC is an ANSI standard for basic space centering.

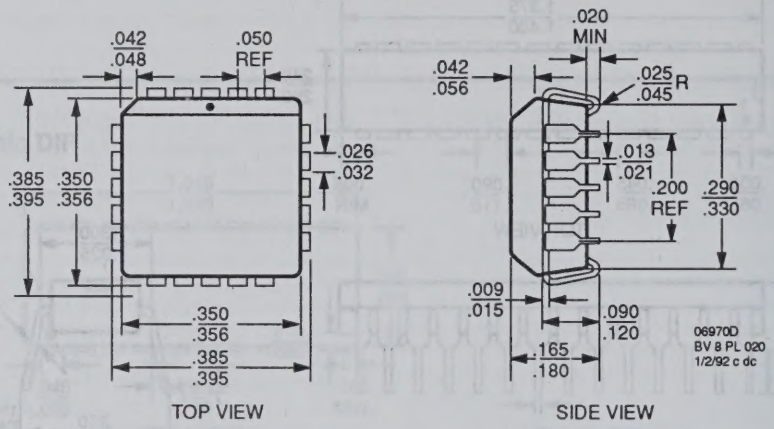
PD 3028
28-Pin 300-mil Plastic SKINNYDIP



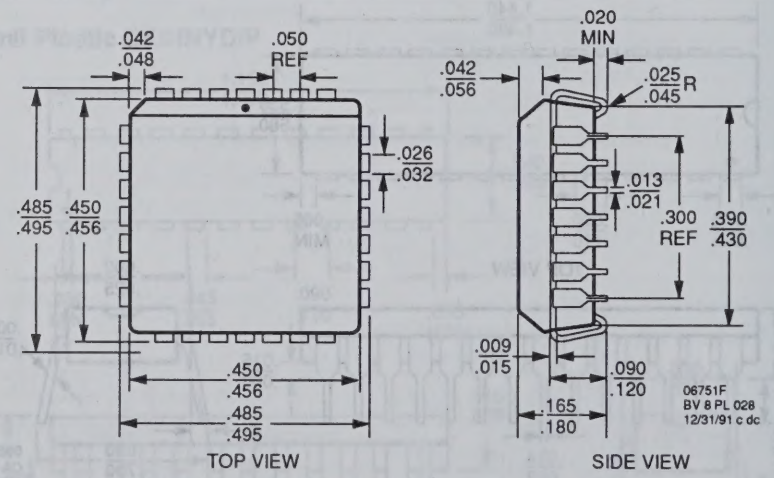
PD 028
28-Pin Plastic DIP



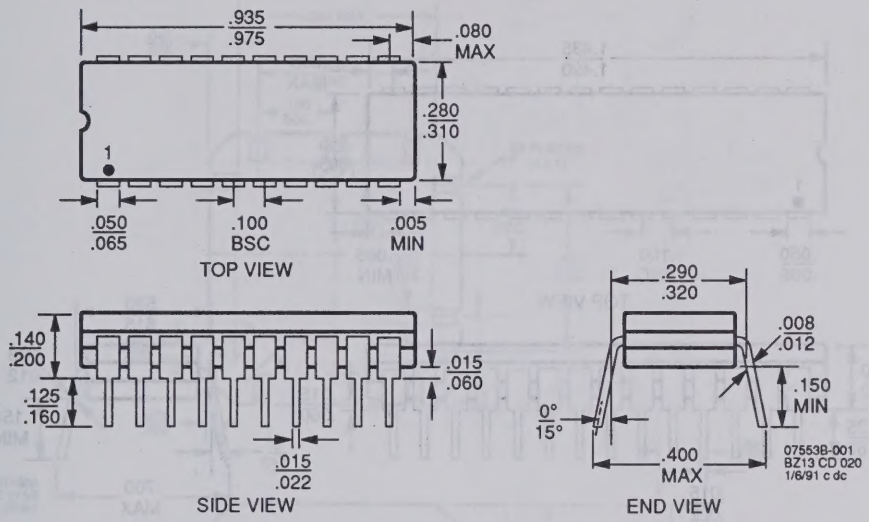
PL 020
20-Pin Plastic Leaded Chip Carrier



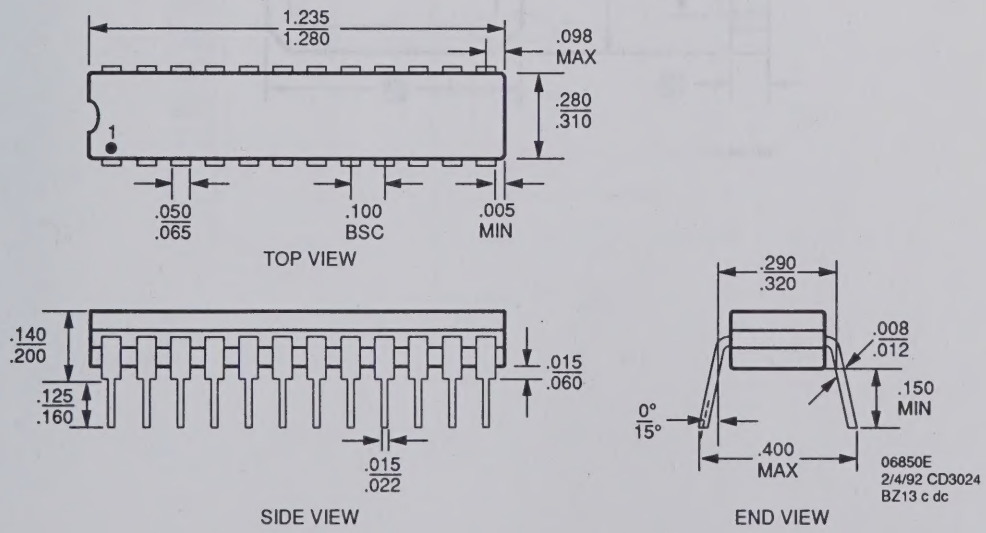
PL 028
28-Pin Plastic Leaded Chip Carrier



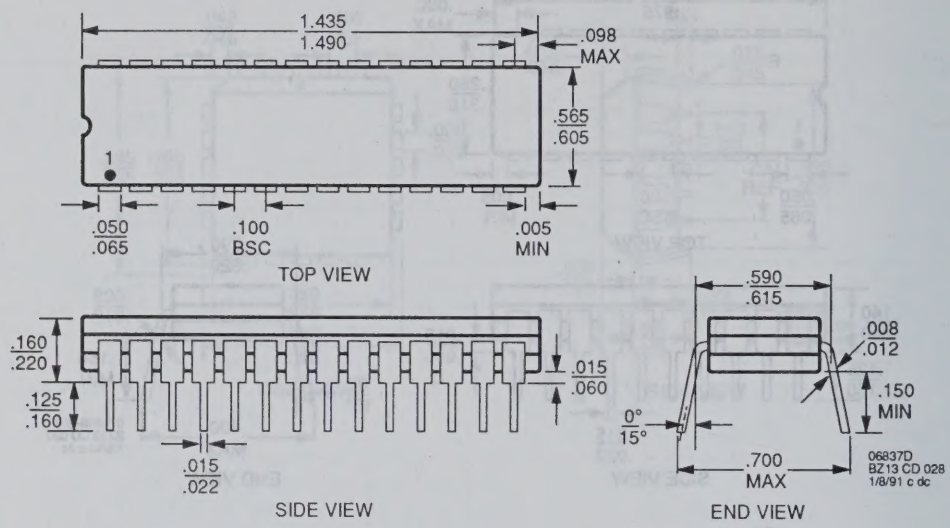
CD 020
20-Pin Ceramic DIP



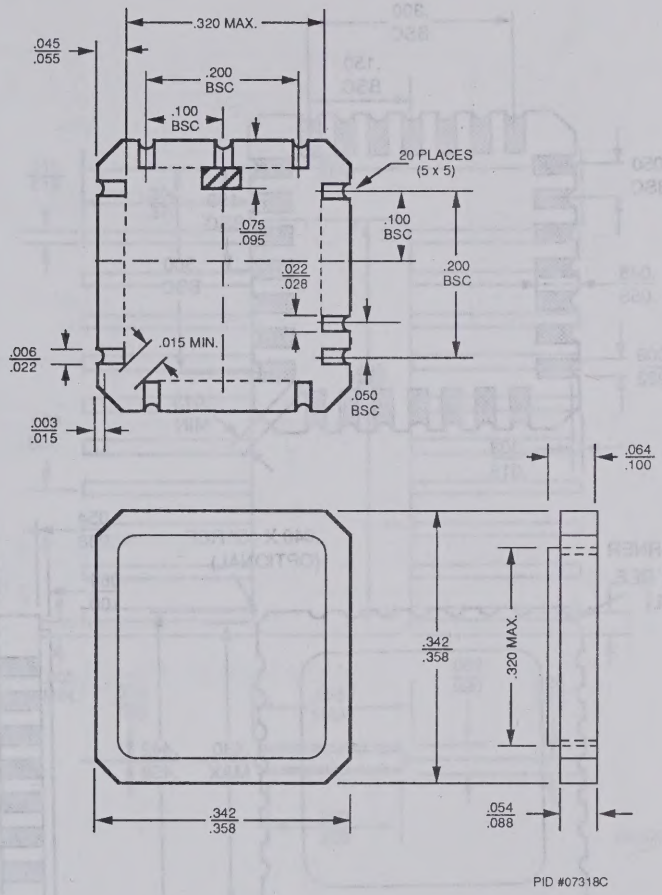
CD 3024
24-Pin 300-mil Ceramic SKINNYDIP



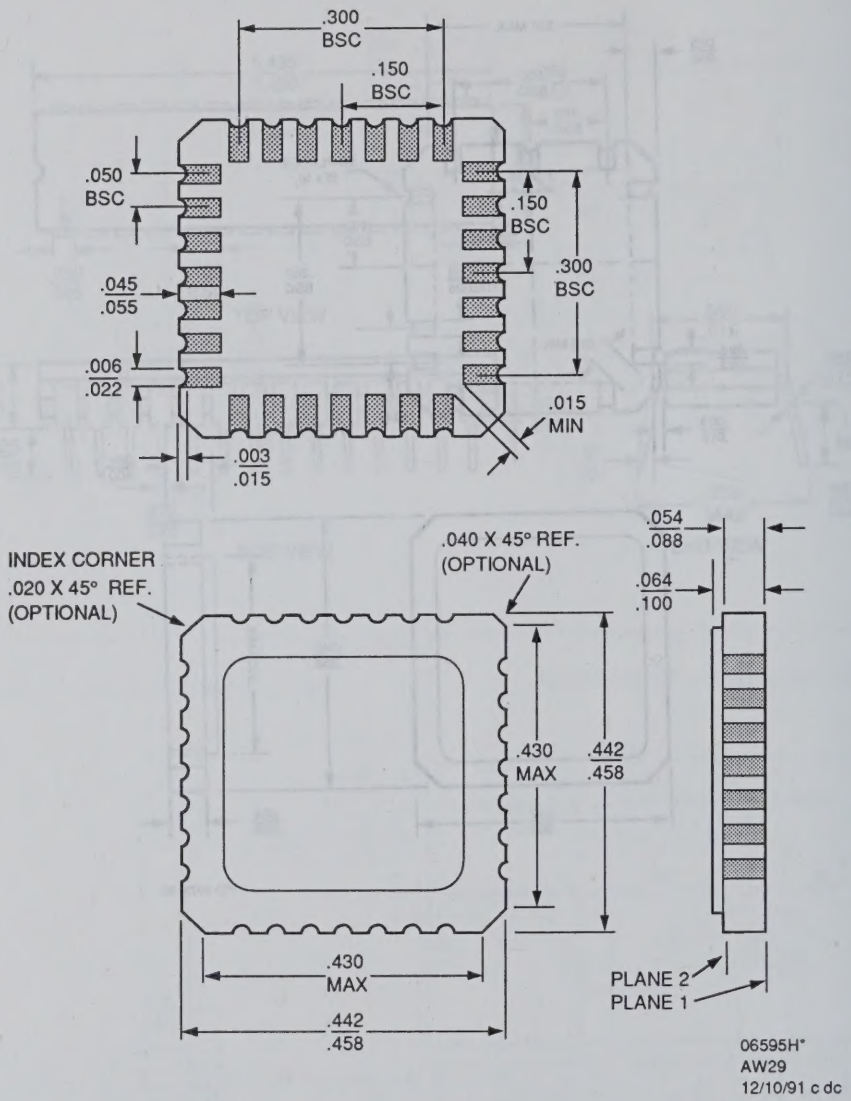
CD 028
28-Pin Ceramic DIP



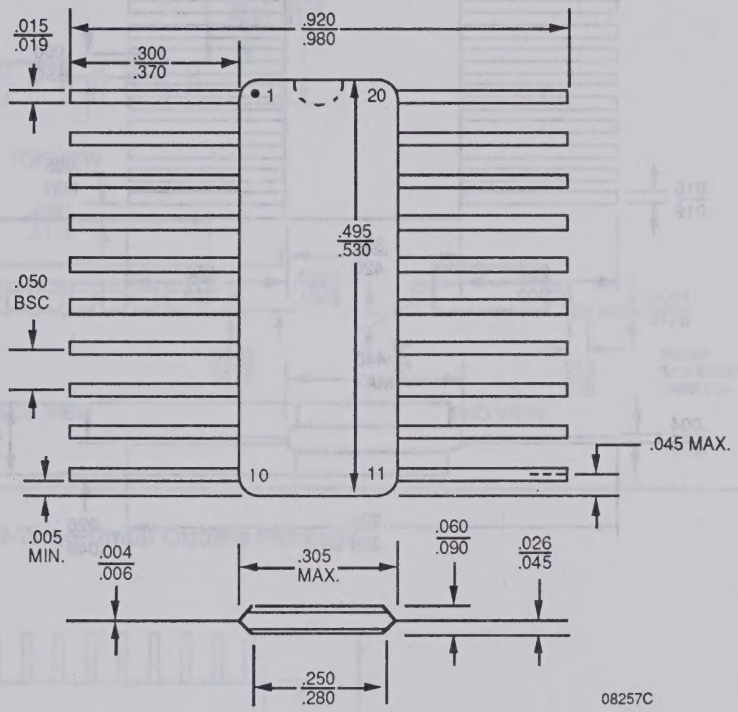
CL 020
20-Pin Ceramic Leadless Chip Carrier



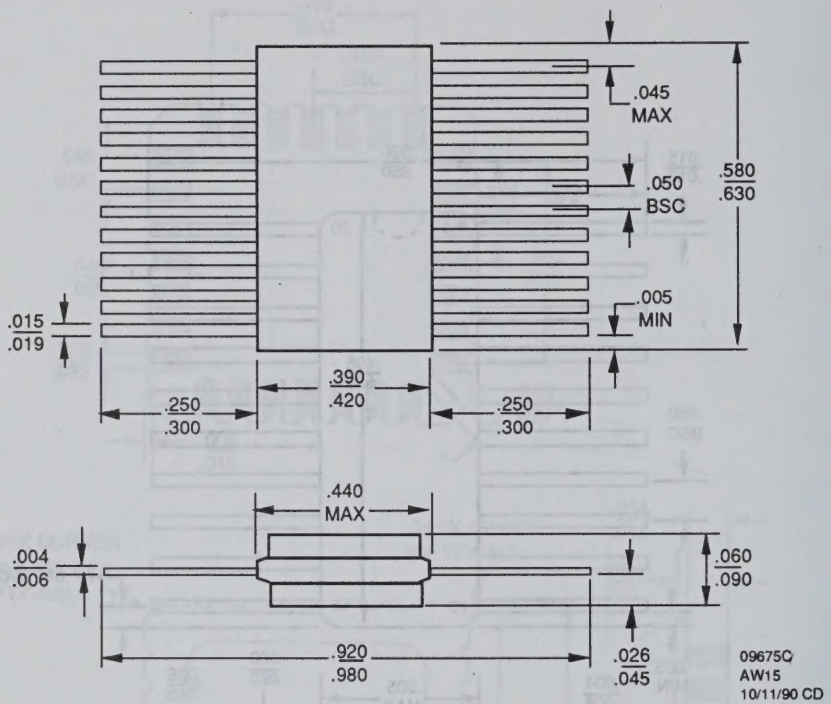
CL 028
28-Pin Ceramic Leadless Chip Carrier



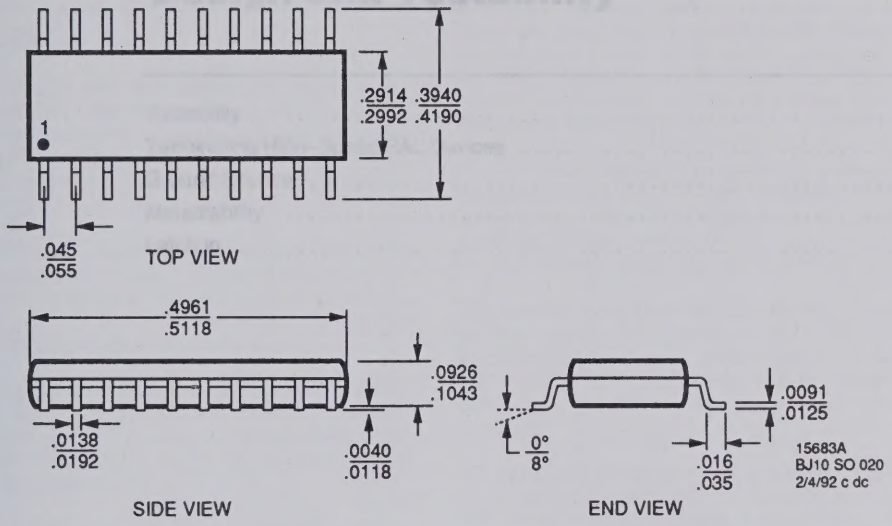
CF 020
20-Pin Ceramic Flatpack



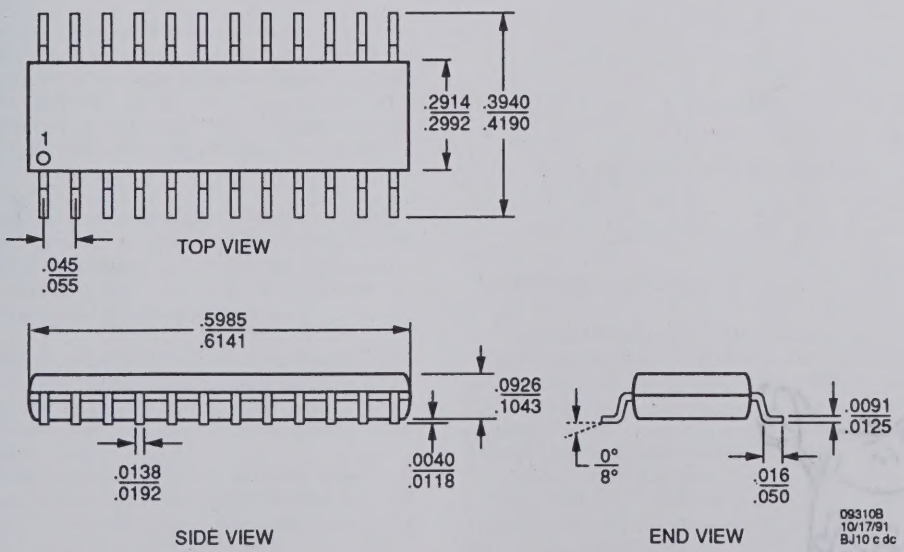
CFL 024
24-Pin Ceramic Flatpack



SO 020
20-Pin Plastic Gull-Wing Small Outline Package



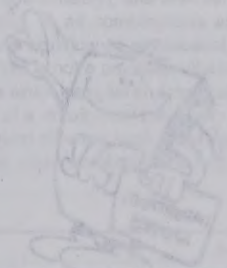
SO 024
24-Pin Plastic Gull-Wing Small Outline Package

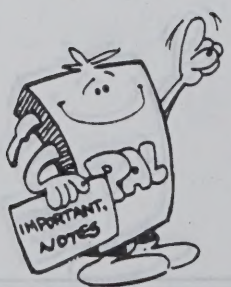


IMPORTANT
NOTES

CHAPTER 4
Design and Testability

Testability 4–3
Terminating High–Speed PAL Devices 4–22
Ground Bounce 4–31
Metastability 4–34
Latchup 4–36




IMPORTANT
NOTES

Testability

INTRODUCTION

With digital logic design, it is all too easy to design a circuit which merely implements a specified function. When production starts it is suddenly found that the circuit cannot be tested, or perhaps that tests cannot be performed economically. Dealing with this situation can, at the very least, have a negative impact on the introduction of the system into the marketplace.

Potential headache can be avoided by taking test issues into consideration during the initial design. Instead of just designing a circuit which implements a specified function, which is the bare minimum that must be accomplished, that function needs to be implemented in a manner which can be tested.

The purpose of this section is to establish the notion of testability and its importance, and then to provide ways of avoiding the most common untestable circuits. The issues will be discussed primarily in the context of logic design in PLD's, although they are also relevant for general logic design.

In addition, test vectors will be reviewed. Various kinds of vectors are mentioned, and the general tools available for vector generation will be summarized.

Defining Testability — A Qualitative Look

A completely testable design is one in which any and all device faults can be systematically detected.

First note that the issue is one of devices, not designs. The design itself must work as specified; that is the main job of the design engineer. Once the design is implemented in a device, the issue is how to test the device to make sure that the design has been correctly implemented. Throughout this paper, then, it will be assumed that a particular design works as is; we will just be addressing its testability.

The easiest and most effective means of testing a circuit is through a systematic series of tests. A random set of tests may also do well, but does not yield much information regarding the testability of a circuit itself. No number of random (or systematic) vectors can test an inherently untestable circuit.

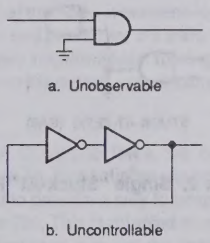
In order to be able to perform a systematic test sequence, every part of the circuit under test must be accessible, so that it can be controlled. Only then can each node be forced high or low as needed. This is essentially a requirement of complete *controllability* of the circuit.
In order to be able to detect faults every part of the circuit must also be visible to the outside world, so that the results of each test can be observed. In this manner, each node can be inspected to determine its logic level. This requires complete *observability*.

These are, of course, the age-old issues of controllability and observability, which are as important for digital logic circuits as they are for so many other kinds of systems. If any portion of a circuit is uncontrollable or unobservable, then the testability of the entire circuit is compromised.

Figure 1 shows a couple of completely untestable circuits. The integrity of the top input in Figure 1a can never be verified. No matter whether it is shorted to ground, to V_{CC}, or whether it is functioning correctly, the output will be the same. That is to say, any faults on the top input cannot be observed at the output.

The circuit in Figure 1a would appear pretty useless as is. It is possible, however, that instead of being directly grounded, the second input may be driven by some distant signal, possibly on a different PC board, which happens to be a a logic low. If you cannot bring this line to a logic high, then it might as well be grounded.

The circuit in Figure 1b essentially has no input. This circuit can be thought of as a latch, but there is no way to change its logic state. Therefore, it is completely uncontrollable.



a. Unobservable

b. Uncontrollable

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Figure 1. Untestable Circuits

Quantifying Testability

In theory, if we want to quantify the testability of a given circuit, we might first attempt to make a list of all possible things that could go wrong with a circuit (no matter how unlikely), and then verify that all such "faults" can be tested, in all combinations and permutations. But for a circuit of any significance whatsoever, it will rapidly become apparent that this is not a practical solution. What we need instead is a measure which can give an empirically reliable indication of the testability of a circuit, or of the quality of a given set of tests. There are several different such measures, but the most popular of these is the *single stuck-at faults* model.

There are several ways of analyzing circuits for single stuck-at faults. For very large circuits, various *testability analysis* schemes have been developed. However, for smaller circuits, especially of the size that would be put into a PLD, the more common method uses simulation.

Simulating Single Stuck-At Faults

A given circuit is first simulated. The quality of the simulation is important; the more complete the simulation the better. A thorough simulation can then serve as a benchmark test sequence later. In this way, the fault simulation procedure also allows us to measure the quality of a given simulation, or set of tests, in addition to the testability of the circuit.

The results of the simulation are recorded. Next, one node in the circuit is modeled with a *"stuck-at" fault* — either *stuck-at-one* (SA1) or *stuck-at-zero* (SA0), as shown in Figure 2. The circuit is now resimulated. If the simulation results of the modified circuit are different from the simulation results of the good circuit, then the fault was detected. If not, then we have a faulty circuit which appears to operate correctly.

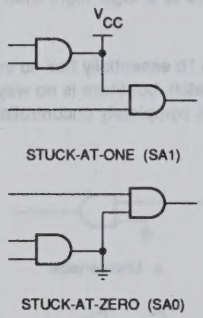

Figure 2. Single "Stuck-At" Faults

This procedure is repeated for each node, one node at a time (hence the name "single" stuck-at faults). The nodes are modeled with both SA1 and SA0 faults, so that for N nodes, we will have 2N simulations. If of those 2N simulations, D of them produced simulation results different from those of the original circuit, then we say that this simulation tested this circuit with a test coverage of D/(2N)*100%. Whereas this specifically tests only for single faults, experience shows that it is also a good test for multiple stuck-at faults.

Undetected Faults

Why are some of the faults not detected? For simple combinatorial logic, there are two basic reasons: either the simulation was not complete enough to find the fault, or the circuit itself cannot be tested for the fault. So when an undetected fault is located, the first step taken is to add vectors to the simulations which will exercise the node being tested. By doing this, we gradually improve the quality of the simulation, and thus the quality of the test sequence that we can use in production.

It is possible that certain nodes will have undetectable faults for which no new vectors can be added. These are the result of an untestable design. It is the joint job of the test and design engineers to generate a test sequence that is as complete as possible. It is the design engineer's responsibility to provide a circuit which is testable. If both of these responsibilities are carried out, the result will be a testable circuit which can be tested with an exhaustive test sequence. This will yield the highest quality system. Note, however, that the overall responsibility is shared between the design and test engineers.

Needless to say, this process of analyzing the testability of a circuit is not done all by hand; software aids are used. There are many different kinds of programs that run on many different kinds of systems, ranging from PCs to workstations to mainframes. Some of them are standalone programs; others are integrated into larger overall environments. Their specific capabilities also vary, but in general, they can simulate a given circuit with a given set of vectors; analyze the test coverage that the vectors provide for the circuit; and generate new tests, either from scratch or by improving on the coverage of a few manually generated "seed" vectors. Most can also point out potential problems areas of a circuit, such as race conditions and logic hazards.

Finally, one frequently asked question is "So what if there is a fault that can never be detected. Who cares?" Theoretically, this question is not unreasonable. However, most companies will not feel comfortable telling a customer "We only tested half of the system, but if anything goes wrong with the other half, you'll never notice it." In addition, as will be seen, many untestable circuits occur as a result of poor design practices.

Testability issues for sequential circuits have implications far beyond the test bed. Indeed, failure to take these issues into account can greatly affect the normal performance of a system. The key for state machines is controllability. The challenge is to make all elements of the circuit controllable, both for testing and for general functionality.

Designing Testable Combinatorial Circuits

All of the previous procedures dealt mostly with the ways in which existing circuits are treated. However, if a finished circuit is found to be untestable, then it must be redesigned for testability. An easier approach is to design for testability from the beginning. Unfortunately there is no direct recipe for a testable design. There are, however, many common ways of making a circuit untestable. Most of this section is devoted to pointing out such problems.

The simplest kind of problem is *redundant logic*. Figure 3a shows one such circuit. It has a purely redundant product term. If the output of either of the product terms is stuck low, for any reason, then as long as the other product term is good, the fault will never be visible at the output.

This may initially look like a benefit, since we have what we could call a "primary" circuit with a "backup." One can cover up some of the failures of the other (but not all failures). If this kind of redundancy is truly desired, this is not the way to achieve it. When you ship out this circuit, you do not know if you really have a working primary and backup. The primary may already be malfunctioning; since it was never tested, you will never know. If you

want useful, reliable redundancy, test circuitry must be added, as in Figure 3b, so that each part of the circuit can be independently tested.

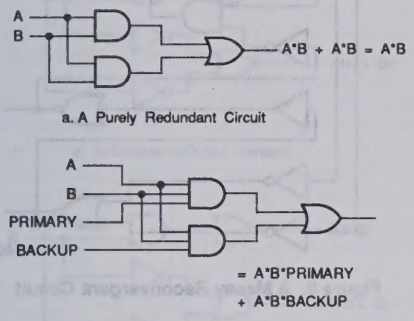

Figure 3. Making Redundancy Testable

Figure 4 shows another redundant circuit. Although the product terms are not identical, the larger AND gate is really redundant. Any stuck-low faults at the output of this gate are not detectable.

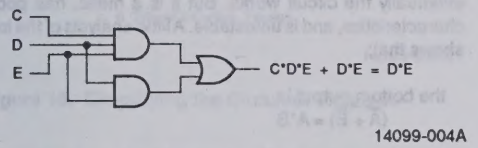

Figure 4. Circuit with a Redundant 3-Input AND Gate

Reconvergent Fanout

Redundant logic is a special case of what is called *reconvergent fanout*. This is a term that refers to circuits that have inputs splitting up, going through independent logic paths, and then reconverging to form a single output, as shown in Figure 5. When this happens, it is very easy to introduce untestable nodes. It may not be easy to identify where such nodes are.

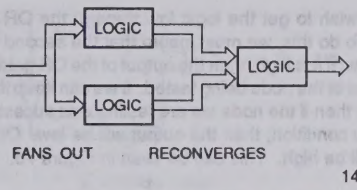

Figure 5. Reconvergent Fanout

Figure 6 is an example of a reconvergent circuit. The inputs are shared between two different product terms, which are eventually summed. This circuit appears harmless enough, but it turns out that the node indicated by "SA1" cannot be tested for a stuck-at-one condition. In other words, there is no way that we can guarantee that that node is operating correctly.

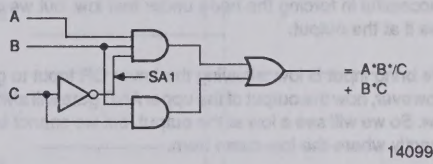

Figure 6. A Reconvergent Circuit with an Untestable Node

It is worth analyzing this circuit a bit more closely. This will give some insight into the kinds of analyses that are necessary when evaluating circuits and generating tests, and into the ways in which untestable nodes are created.

If we wish to prove that the node in question is not stuck high, then we must force it low and prove that we were successful in doing so. Thus we have two requirements: forcing the node low, and seeing the logic low on the output—controlling and observing the node.

First we raise input C high to force the node to a logic low condition, as in Figure 7a. This satisfies our controllability requirement. Next we need to provide a way to propagate this logic low to the output (Figure 7b). This is referred to as *sensitizing a path* to the output. The first step is to get the logic low past the AND gate. But if either input A or B is low, then the output of the AND gate will be low regardless of the node being tested. Thus we must force both A and B to a logic high, so that if there is a low on the output of the AND gate, we will know for sure that it came from the node we are testing. This is shown in Figure 7c.

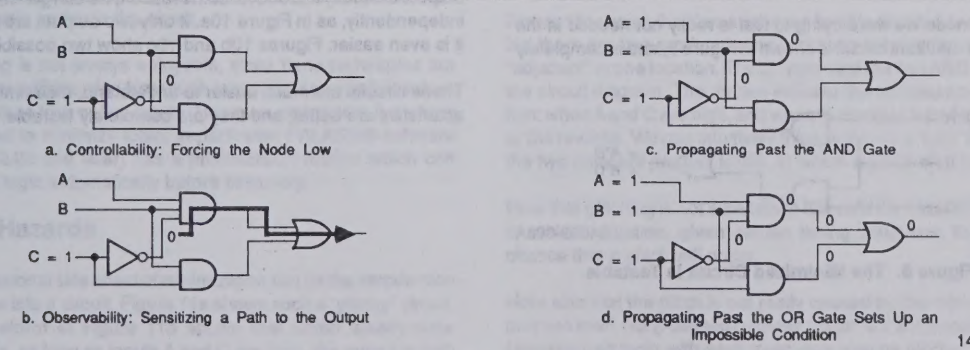

Figure 7. Analyzing Testability

Next we wish to get the logic low through the OR gate to the output. To do this, we must insure that the second OR input is always low; if it is high, then the output of the OR gate will be high regardless of the node being tested. If we can keep the lower OR input low, then if the node we are testing was sucessfully forced into a low condition, then the output will be low. Otherwise the output will be high. This can be seen in Figure 7d.

How do we keep the lower OR input low? By making the output of the lower AND gate low, which can be done by setting one of its inputs low. However, we have already required that all of the inputs be high. Thus we have required a set of conditions that cannot be met. One of three things will result:

1. The lower AND gate has both inputs high, and therefore keeps the lower OR input high. In this case, we may have been successful in forcing the node under test low, but we cannot see it at the output.

2. We bring input B low, allowing the lower OR input to go low. However, now the output of the upper AND gate will always be low. So we will see a low at the output, but we cannot be sure exactly where the low came from.

3. We bring input C low, allowing the lower OR input to go low. However, now we are no longer forcing the node under test low.

So we can either force the node low, but cannot see the low at the output; or, we can see a low at the output but cannot be sure of its source; or, we cannot force the node itself low. In any case, we will never be able to guarantee that the node under test is not stuck high.

Note that the two "independent logic blocks" which generate the signals that eventually reconverge are testable by themselves; they are just AND gates. It is only when we hook them together via the OR gate that the overall circuit becomes untestable. Thus *the testability of individual portions of a circuit does not guarantee that the entire circuit will be testable when the testable pieces are all connected.*

We can minimize this circuit using the following steps:

$$A*B*\overline{C} + B*C = A*B*\overline{C} + B*C + A*B*B \text{ (by consensus)}$$
$$= A*B*\overline{C} + B*C + A*B$$
$$= A*B + B*C$$

Thus the node we were trying to test is really not needed in the logic. The resultant circuit is shown in Figure 8, and is completely testable.

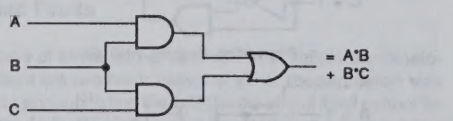

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Figure 8. The Minimized Circuit Is Testable

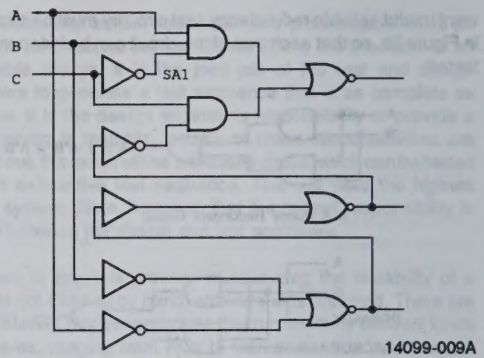

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Figure 9. A Messy Reconvergent Circuit

Not all reconvergent circuits are so simple. Figure 9 shows a more complicated reconvergent circuit. Here some signals have to travel through several levels of logic to reach their final destination. This introduces considerable skew into the circuit, and will produce glitches on the outputs during certain transitions. In addition to this, there is again a stuck-at-one fault that cannot be tested.

Circuits like this can result from the design iteration process, as a designer tries to debug a circuit. By adding this and that, eventually the circuit works. But it is a mess, has poor timing characteristics, and is untestable. A little analysis of the logic itself shows that:

the bottom output is
$$\overline{(\overline{A} + \overline{B})} = A*B$$

thus the middle output is
$$\overline{(A*B)} = \overline{A} + \overline{B}$$

which makes the top output
$$\overline{(A*B*\overline{C} + C*\overline{(\overline{A} + \overline{B})})} = \overline{(A*B*\overline{C} + A*B*C)}$$
$$= \overline{(A*B)}$$
$$= \overline{A} + \overline{B}$$

That is, the top two outputs are actually the same, and the third output is just the inverse of the top two. As convoluted as the original circuit looks, the logic itself is actually trivial. So if three outputs are really needed for some reason, we can generate them independently, as in Figure 10a. If only two outputs are needed, it is even easier. Figures 10b and 10c show two possibilities.

These circuits are much easier to understand, their timing characteristics are better, and they are completely testable.

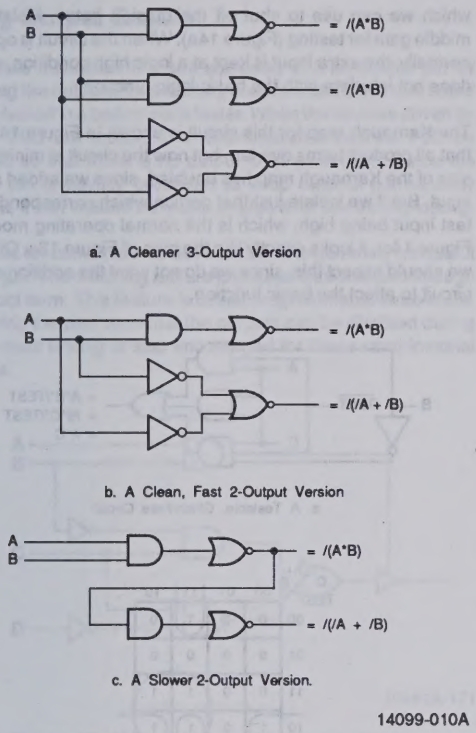

Figure 10. Simplifying the Circuit of Figure 9.

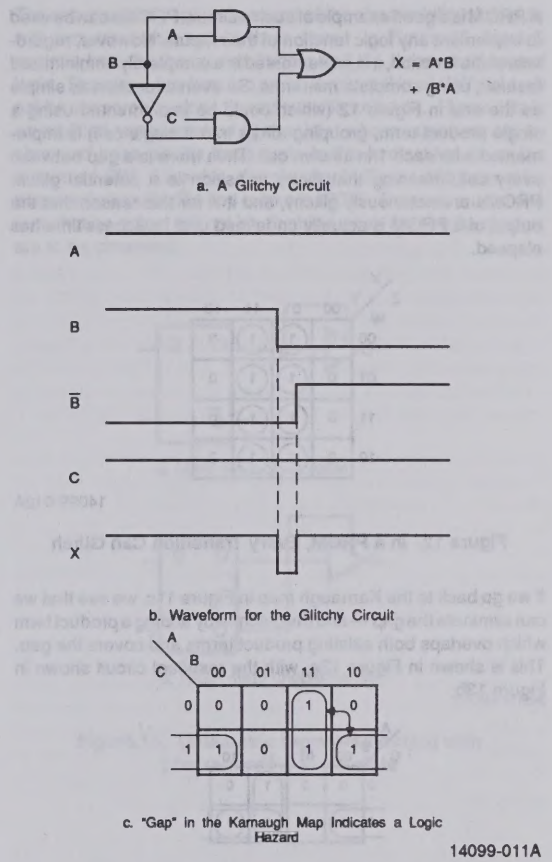

Figure 11. Examining a Glitchy Circuit

The Importance of Minimization

The common factor behind all of the untestable circuits we have examined is the fact that all of them were not minimal. By minimizing the logic, we made the circuits testable. This is true in general: *UNMINIMIZED LOGIC CANNOT BE FULLY TESTED.*

Very often, especially when designing with PLDs, an attempt is made to minimize logic only to the point where it fits into a particular PLD. Any further minimization is considered an academic waste of time. This is a grave misconception. Getting rid of all extra product terms, and eliminating all extra literals on the remaining product terms has real value. Failing to do so will result in untestable nodes in the circuit.

Minimizing is not always enjoyable, since hand techniques are usually too tedious, and Karnaugh maps are essentially useless for more than four or five inputs. However, computers have long been used to minimize logic. In particular, PALASM® software (version 2.22 and later) has a minimization routine which can minimize logic automatically before assembly.

Logic Hazards

One occasional side effect of minimization can be the introduction of *glitches* into a circuit. Figure 11a shows such a "glitchy" circuit. The waveform in Figure 11b shows that under steady-state conditions, as long as inputs A and C are high, the output is high regardless of B. However, as B changes from high to low, causing the top product term to shut off and the bottom one to turn on, the inverter adds a bit of delay to the path that will turn on the lower product term. Thus the top term may shut off before the bottom one gets a chance to turn on. In this case, we have two logic low signals going into the OR gate, giving a low on the output. As soon as the lower product term turns on, the output goes back high, but not before the appearance of the high-low-high glitch.

Figure 11c shows the Karnaugh map for this circuit. It is minimal, but there are two product terms which do not overlap; they are "adjacent" in one location. These represent the two AND gates in the circuit diagram. The arrows indicate the troublesome transition: when A and C are high, and when B changes from high to low or the reverse. We can intuitively think of this as a "gap" between the two adjacent product terms, in which a glitch may occur.

Note that glitching is not a certainty. It is called a *hazard* because in certain situation, given certain timing situations, there is a chance that a glitch will occur.

Note also that the glitch is not really caused by the minimization process itself, but is caused by these "gaps" in the Karnaugh map. Unminimized logic with such gaps may also be glitchy.

A PROM is a good example of such a circuit. PROMs can be used to implement any logic function of their inputs. However, regardless of the function, it is implemented in a completely unminimized fashion, using complete minterms. So even a function as simple as the one in Figure 12 (which could be implemented using a single product term, grouping all 1's into a single cell) is implemented with each 1 in its own cell. Thus there is a gap between every cell, meaning that every transition is a potential glitch. PROMs are notoriously glitchy, and it is for this reason that the output of a PROM is actually undefined until its access time has elapsed.

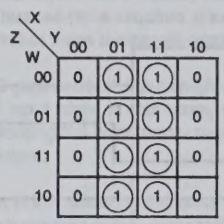

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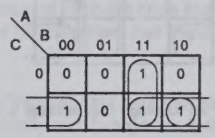
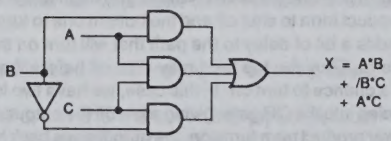
Figure 12. In a PROM, Every Transition Can Glitch

If we go back to the Karnaugh map in Figure 11c, we see that we can eliminate the gap — and the glitch — by adding a product term which overlaps both existing product terms and covers the gap. This is shown in Figure 13a, with the resultant circuit shown in Figure 13b.



a. A Redundant Product Term Can Eliminate the Glitch



b. A Glitch-Free, but Untestable Circuit

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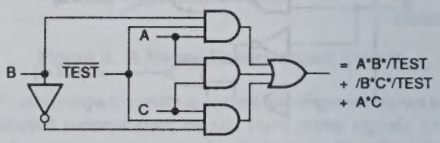
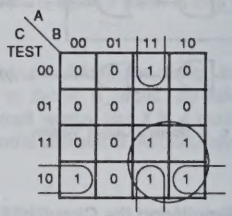
Figure 13. Eliminating Glitches

This circuit is no longer glitchy. Unfortunately, it is also no longer testable, since we have added in a redundant product term that cannot be tested (try it yourself). In order to have a circuit that is both testable and glitch-free, we must add a test input to the circuit which we can use to shut off the outside gates, isolating the middle gate for testing (Figure 14a). When the circuit is operating normally, the extra input is kept at a logic high condition, where it does not interfere with the basic logic function.

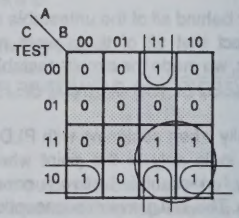
The Karnaugh map for this circuit is shown in Figure 14b. Note that all product terms overlap, but now the circuit is minimal. The size of the Karnaugh map has doubled, since we added another input. But if we isolate just that portion which corresponds to the test input being high, which is the normal operating mode (see Figure 14c), it looks exactly like the map of Figure 13a. Of course we should expect this, since we do not want the addition of a test circuit to affect the basic function.



a. A Testable, Glitch-Free Circuit



b. Karnaugh Map



c. Karnaugh Map Showing Non-Test-Mode Portion

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Figure 14. Making a Glitch-Free Circuit Testable

Thus, in general, these types of glitches can be eliminated first by adding some redundant logic to get rid of the gaps in the Karnaugh map, and then by adding a test input to make the circuit testable.

Using Output Enable

Most state machine PLDs are equipped with an enable pin for disabling the outputs. This is a key feature when the circuit board is to be tested in a bed-of-nails tester. When the devices driven by by the PLD are tested, it is recommended that the PLD be disabled so that there is no output level contention. Since the enable pin is usually grounded to keep outputs permanently enabled, it can instead be made available for use during testing.

Note that for combinatorial devices, there is generally no output enable pin. The disabling feature is instead implemented through a product term. This feature is called programmable three-state. Designing the part such that the outputs can be disabled during bed-of-nails testing is also encouraged for these combinatorial designs.

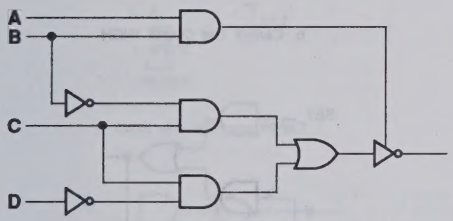

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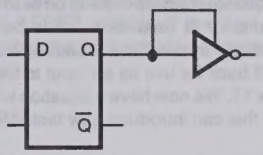
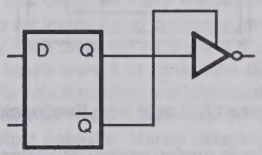
Figure 15. Untestable combinatorial circuit with programmable three-state

The user must be especially aware of the observability of outputs with programmable output three-state. In Figure 15, input B controls both the basic circuit logic and the three-state control logic. Therefore, any function which involves B in a LOW state will not be observable, since the output will not be on. Figure 16a is a simplified representation of a register whose output cannot be observed because the three-state buffer is disabled when the output is LOW. Likewise, the circuitry in Figure 16b cannot be observed when the flip-flop output is HIGH. The user must make sure that an output will not be disabled when the results of a test are to be observed.



a. LOW state observable



b. HIGH state unobservable

14099-015A

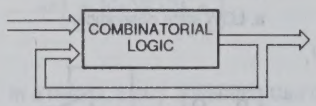
Figure 16. Untestable registered output with programmable three-state

Designing Testable Sequential Circuits

The design of sequential circuits involves considerations above and beyond those required for simple combinatorial circuits. Latches and oscillators are circuits which appear combinatorial, but which use feedback to introduce sequential properties. State machines use flip-flops and feedback to generate what can be complex sequential circuits.

Feedback

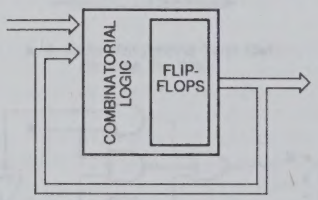
Whereas combinatorial circuits depend only on the conditions of present inputs, *sequential* circuits depend on both present conditions and past behavior to determine future behavior. This is made possible primarily by *feedback*. Feedback takes an output signal and routes it back for use as an input to the same circuit, as shown in Figure 17. We now have a situation where an output depends on itself; this can introduce new testability problems.



14099-016A

Figure 17. Logic with Feedback

Most sequential circuits (under varying circumstances also called *state machines*, *finite state machines*, and *sequencers*) make use of *flip-flops* as memory elements. These memory elements serve to remember a past condition (called a *state*) so that a future decision can be made based on it. This state is then fed back as input. With PLDs, the flip-flops and combinatorial logic are contained within a single device, as shown in Figure 18.



14099-017A

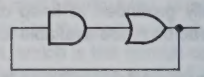
Figure 18. Structure of a Sequential PLD

Of course, the effects of feedback may have to be considered even when there are no flip-flops. The circuit in Figure 17 has feedback, but has no flip-flops. Such a circuit will either function as a *latch* or as an *oscillator*, as will be seen.

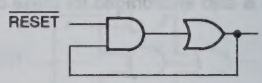
Before we look into the special needs of circuits with feedback, bear in mind that all of the testability criteria discussed for combinatorial logic still hold. The blocks of combinatorial logic shown in Figures 17 and 18 must be testable by themselves. What we will discuss here are issues which must be considered in addition to the issues involving combinatorial logic.

Latches

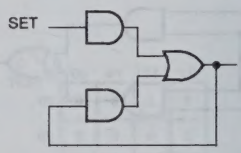
A combinatorial logic circuit which uses positive feedback is a latch. The simplest possible latch is shown in Figure 19a. The output is fed back as an input in its TRUE form. This means, of course, that the output will stay at its present level; hence the name "latch."



a. Completely Uncontrollable



b. Cannot Set Output HIGH



c. Cannot Reset Output LOW

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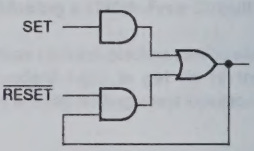
Figure 19. Uncontrollable Latches

The circuit as shown is clearly not useful, since it will always remain in its power-up state. If another input is added, as in Figure 19b, a HIGH output could be made to go LOW by setting the $\overline{\text{RESET}}$ input LOW. However, once the output goes LOW, there is no way to make it go HIGH again. Likewise, the circuit could be modified as in Figure 19c. Now a LOW output can be made HIGH by setting the SET input HIGH. However, once HIGH, the output can never be made to go back LOW.

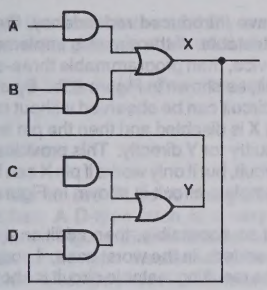
Controllable latches

For a latch to be useful, it must be completely controllable. The previous latches cannot be completely controlled. In order for a latch to be controllable, it must have both SET and RESET controls, as shown in Figure 20.



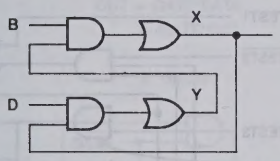
14099-019A

Figure 20. A Controllable Latch



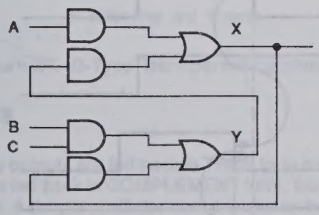
X = A
+ B*Y
= A
+ B*(C + D*X)
= A
+ B*C
+ B*D*X
SET
RESET

a. Latch with SET and RESET



X = B*Y
+ B*D*X
RESET

b. Latch with RESET Only



X = A + Y
= A
+ B*C
+ X
SET

c. Latch with SET Only

14099-020A

Figure 21. More Complex Latches

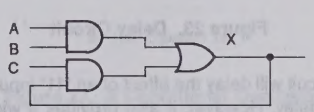
In PLDs, a latch can be detected by simplifying the logic for each function. If an output is a function of itself in TRUE form, then it is a latch. To be controllable,

- product terms containing the feedback should have at least one other direct input in the product (providing RESET control).
- there should be at least one product term with no feedback (providing SET control).

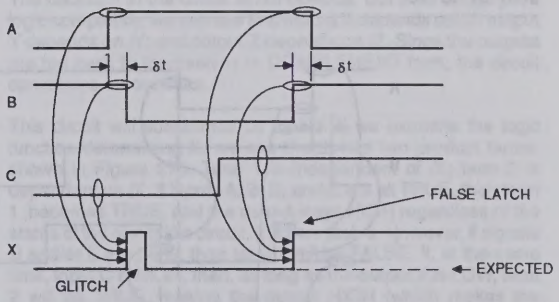
The circuit in Figure 21a provides an example. At first it is not immediately obvious that the circuit is a latch, but when the logic is simplified, we see that indeed it is. It is controllable since it has both SET and RESET controls. If the logic were as shown in Figures 21b or 21c, the latch would be uncontrollable under some circumstances.

Latch hazards

The circuit of Figure 20 can be generalized to have several inputs on both the set and reset controls. Such a circuit is shown in Figure 22. In this case, we have two inputs on the set AND gate. If the two set inputs A and B change from 0 and 1 to 1 and 0, respectively, then there will be a glitch or a false latch at the output if both inputs were 1 at some time during the transition (Figure 22). For this transition, it is important to make sure that the 1-0 transition be made before the 0-1 transition to avoid anomalous output behavior. Merely delaying one input will not help, since it will delay both rising and falling transitions.



a. Circuit



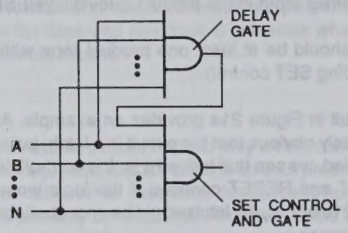
b. Glitch and False Latch

14099-021A

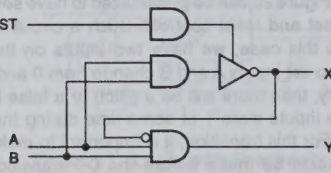
Figure 22. A Latch with More Complex SET Logic

The simplest solution to this problem is the use of an edge-triggered flip-flop to synchronize the signals. This will eliminate any such glitches. If a flip-flop cannot be used, it is possible to delay reaction to a "11" condition to make sure that such a condition is not transitory. A circuit that accomplishes this is

shown in Figure 23a. This is relatively efficient in that only one delay circuit is required regardless of the number of inputs used on the set control (within the limits of the size of the AND gate). It will require an extra output on a PAL device.



a. Circuit Which Delays "11...1" signals



b. Testable Delay Circuit

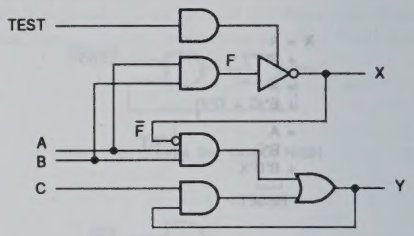
14099-022A

Figure 23. Delay Circuit

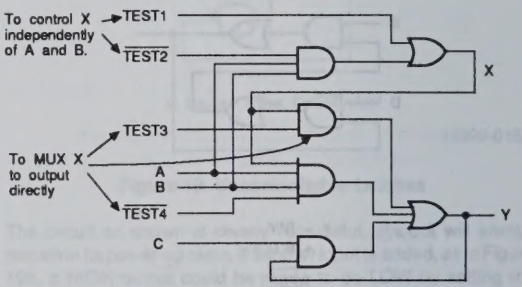
This delay circuit will delay the effect of an "11" input by an extra propagation delay. However, it also provides a window of one propagation delay which will screen out any transitory "11" conditions that occur within that window. This allows up to one propagation delay's worth of skew between inputs during a transition from "01" to "10."

Because we have introduced redundancy, the circuit must be modified to be testable. If the circuit is implemented in a combinatorial PAL device, then programmable three-state can be used to test the circuit, as shown in Figure 23b. By enabling output X, the redundant circuit can be observed without regard to Y. Then, to test Y, output X is disabled and then the pin is used as an input to drive the circuitry for Y directly. This provides a simple means of testing the circuit, but it only works if pin X can be measured and driven. The complete circuit is shown in Figure 24a.

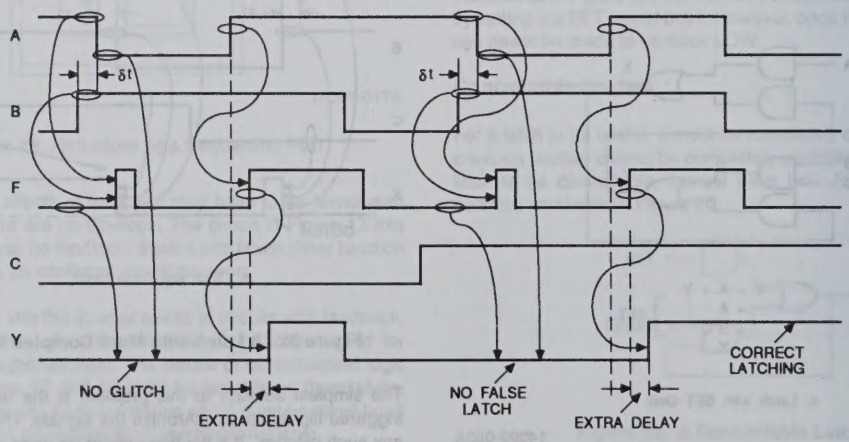
If node X is not so accessible, then additional circuitry and test inputs must be added. In the worst case, if node X is completely inaccessible, the resulting testable circuit is shown in Figure 24b.



a. Complete Latch Circuit



b. Circuit if Node X is Completely Inaccessible



c. Latch Circuit Behavior

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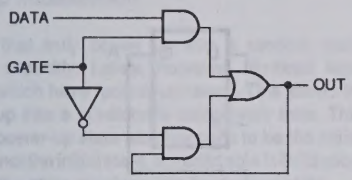
Figure 24. A Testable Glitch-Free Latch

Note that although the three-state capability is not needed, the circuit requires two extra gates, and, worst of all, four test inputs.

Figure 24c shows the behavior of either of the testable glitch-free latches.

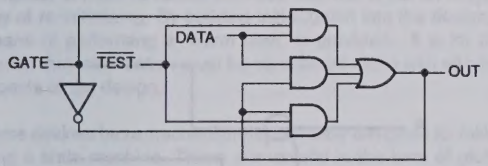
Transparent latches

Many designers like to use PLDs to design standard D-type "transparent" latches. A D-type latch is a very simple circuit, shown in basic form in Figure 25a. As it turns out, however, this is a glitchy circuit of the type discussed in the combinatorial section. The problem is compounded in this case, since, given the right timing, the glitch can actually be latched; the glitching problem is no longer transitory. If this type of circuit is desired, it must be designed to be both glitch-free and testable; the resultant circuit is shown in Figure 25b.



OUT = GATE*DATA
+ /GATE*OUT

a. Glitchy



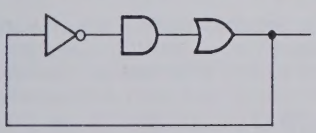
OUT = GATE*DATA*/TEST
+ /GATE*OUT*/TEST
+ DATA*OUT

b. Glitch-Free and Testable 14099-024A

Figure 25. D-Type Transparent Latches

Oscillators

Circuits whose outputs are fed back in TRUE form are latches. If the outputs are fed back in COMPLEMENT form, then the circuit is an oscillator. A simple oscillator circuit is shown in Figure 26.

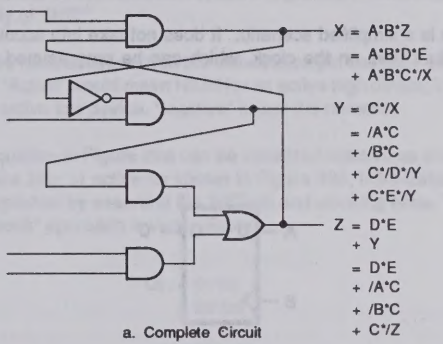


14099-025A

Figure 26. A Simple Oscillator

Latches are very often useful in circuits; oscillators rarely are. Crystals and other specialized oscillators are useful when it is necessary to generate a clock signal, for example. Trying to build an oscillator out of standard logic or PLDs will not yield a very predictable, accurate oscillator; where these circuits occur, it is usually by accident.

An oscillatory circuit may not always be obvious. It also may not oscillate all of the time. The oscillator shown in Figure 26 is uncontrollable; it always oscillates. However, just as we can design controllable latches, we can also design controllable oscillators (on purpose or by accident). This means that there may be an oscillator hidden in the circuit which will sometimes oscillate and sometimes be stable. Such a circuit is shown in Figure 27a.



a. Complete Circuit

X = A*B*D*E TERM 1
+ A*B*C*/X TERM 1

b. The Equation for X

14099-026A

Figure 27. A Conditional Oscillator

Detecting oscillators

The oscillator in the circuit is not obvious. But if we simplify the logic completely, we can see that output X depends on /X; output Y depends on /Y; and output Z depends on /Z. Since the outputs are fed back to themselves in COMPLEMENT form, the circuit constitutes an oscillator.

This circuit will sometimes be stable. If we examine the logic function determining X, we see that it has two product terms, shown in Figure 27b. Term 1 is independent of /X; term 2 is dependent on /X. If inputs A, B, D, and E are all TRUE, then term 1 becomes TRUE, and the output stays HIGH regardless of the status of the rest of the circuit. It is thus stable. However, if signals D and/or E are LOW, then term 1 will be FALSE. If, at the same time, input C is HIGH, then, as long as the output X is LOW, term 2 will be TRUE, making the output HIGH (which makes the product term FALSE, which makes the output LOW, etc.). That is, the circuit oscillates.

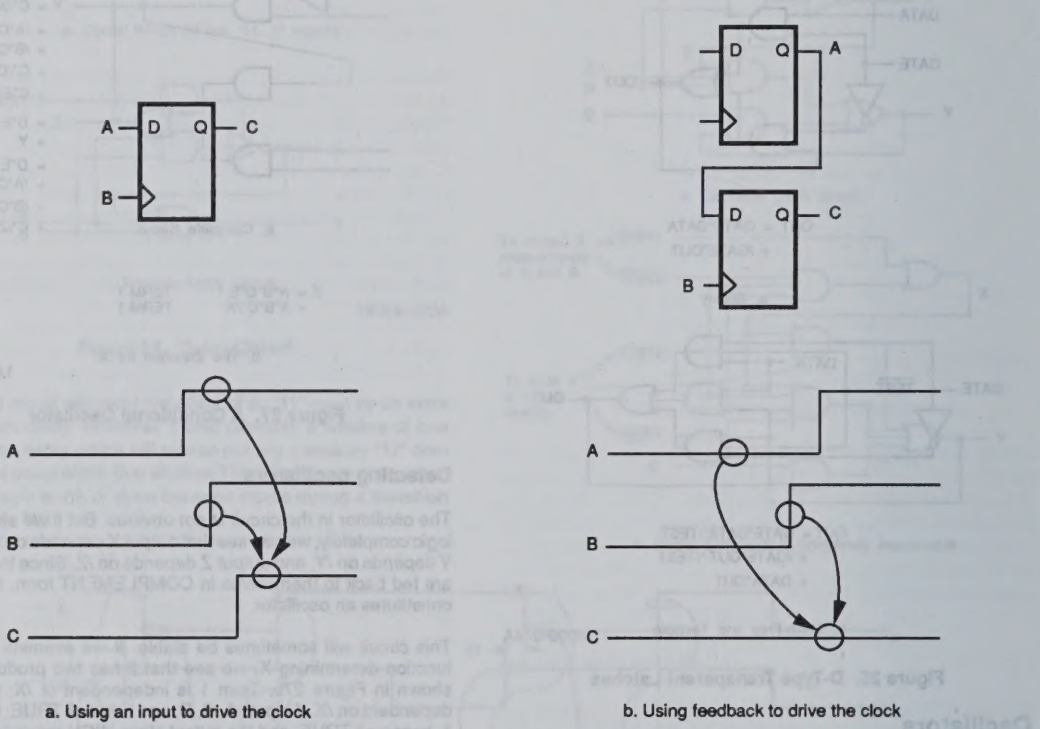
In this manner, we can identify the conditions under which a conditional oscillator will oscillate. The mere presence of an oscillator is usually an indication that the circuit needs to be changed. It may be that the circuit only oscillates under conditions that could never possibly exist. One must be very certain of the impossibility of such a condition, however, if a conditional oscillator is to be tolerated. In addition, a thorough test sequence will usually expose a circuit to conditions that it may never encounter in a real system. Thus oscillators may interfere with the test process even if they do not disrupt the system.

Using a Programmable Clock

When using the programmable clock on an asynchronous device, caution must be exercised with data setup. Refer to Figure 28a, where A and B are primary inputs. One setup time (t_s) after signal A goes active, signal B goes active, clocking signal A into the register. In Figure 28b, B is a primary input but signal A is fed back from another register. In this case it may be harder to ensure that the proper setup time is allowed before signal B is asserted, possibly causing improper information to be clocked into the register.

This is a simplified scenario. It does not take into account the product term on the clock, which can be programmed with a combination of any of the array inputs. A complex clock term can be a hidden source of frequently-violated setup time when feedback terms are used. Always be aware of which input or combination of inputs and feedbacks will clock each register, and calculate setup time backwards from the last input which will assert the clock term. This is the best and probably the easiest method for determining when data must be made available at the D input of the register.

This is an important testability issue because with a programmable clock, the tester may no longer be in control of the clock timing. Automatic test equipment is capable of handling the timing for dedicated clock pins, but the programmable clock feature does not allow the tester the luxury of a single controlled clock pulse.



a. Using an input to drive the clock

b. Using feedback to drive the clock

14099-027A

Figure 28. Using a programmable clock

Designing Testable State Machines

State machines have their own set of controllability issues. These essentially boil down to the concepts of *initialization* and *illegal states*.

State machine initialization

The nature of a state machine is that there is a well-defined sequence of states through which the machine will traverse as it operates. This implies the existence of a "first" state. Of course, these initial states vary from design to design. One obvious problem is the fact that many flip-flops — especially older varieties — do not power up in a predictable state.

Power-up initialization

Flip-flops that truly power up into a random state must be initialized explicitly. Lately, however, flip-flops have become available which have "power-up reset". This allows the flip-flops to power up into a predictable state every time. This is helpful when the power-up state also happens to be the initial state. But even if it is not the initial state, a predictable initialization sequence can bring the state machine into its start-up state.

Unfortunately, such initialization schemes rely on the ability of the device to initialize itself when being powered up. If the system needs to be re-initialized, it will have to be completely turned off and then turned on again. Anyone who has had to turn off a computer in order to reboot will know that this is not an elegant way of re-initializing. By building initialization into the design, a means of performing a "warm boot" is provided. It is for this reason that initialization must be considered along with all other aspects of the design.

Some devices have mechanisms specifically designed for initializing a state machine. These are usually in the form of global preset and reset product terms. By programming the conditions for initialization onto such terms, the device can be re-initialized at any time.

Including initialization in a design

Some of the simpler devices do not have specific provisions for initialization. However, the need is still present in these devices; here the initialization should be included in the design. This is a very simple process; it can be added in after all of the other design details have been worked out. Adding initialization will use up one input pin and potentially one product term on some outputs; this can affect the choice of device for the design.

To provide initialization in an otherwise complete design when Boolean equations are being used:

- determine the start-up state.
- assign each bit as being initialized active or inactive, based on the desired start-up state.
- if a bit is to be initialized inactive, add "/INIT" to every product term for that bit.
- if a bit is to be initialized active, add one product term consisting solely of "INIT."

Here we have assumed that the initialization pin has been called "INIT." "Active" would mean HIGH for an active high device; LOW for an active low device. "Inactive" is just the reverse.

The equation in Figure 29a can be initialized inactive as shown in Figure 29b, or active as shown in Figure 29c. Initialization is accomplished by asserting the INIT pin and clocking once. This "cookbook" approach is very reliable.

```
Q0 := Q1*Q2
    + Q2*/Q3
```

a. Uninitializable

```
Q0 := Q1*Q2*/INIT
    + Q2*/Q3*/INIT
```

b. Initialized Inactive

```
Q0 := Q1*Q2
    + Q2*/Q3
    + INIT
```

c. Initialized Active

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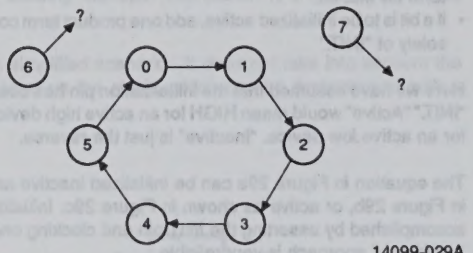
Figure 29. Designing In Initialization

PALASM software also makes it possible to design state machines with a special syntax which essentially allows the state diagram to be transferred directly into a design file. For devices which have no dedicated initialization features, the initialization branches should be explicitly built into the state diagram. The software then performs the remainder of the processing needed.

Illegal states

A state machine is formed by using a set of flip-flops to remember states, and assigning a code to each state. Since there are 2^n different codes that can be assigned to a group of n flip-flops, there is a good chance that some codes may not be used. For example, if a state machine is to have 6 states, 2 flip-flops will not be sufficient; 3 are needed. But 3 flip-flops allow 8 states, which will result in 2 unused states (see Figure 30).



14099-029A

Figure 30. Illegal States

Assuming that the state machine has been designed correctly, there is no reason why these extra states should ever be entered; therefore they are called "illegal" states. Unfortunately, situations do occur, thanks to noise and other unpredictable occurrences, which result in the state machine being in an illegal state. When this happens, the immediate need is to return to a normal sequence of states: *there must be a predictable means of getting from any illegal states into a legal state.*

Illegal state recovery is a controllability issue which actually affects functionality more than it affects testability. But the concepts used for functionality and testing are so closely related that it is worth treating here.

Recovering from illegal states

There are three basic ways to get out of an illegal state:

- re-initialize
- make sure that one can continue clocking until the machine recovers
- design the machine such that the start-up state is reached from any illegal state in one clock cycle, independent of any conditional inputs

Of course, re-initializing will take the machine back into its start-up state from any state, legal or illegal (Figure 31). The disadvantage here is that outside control is needed to force initialization.

Very often, a path will exist which eventually takes the state machine back into a normal sequence (Figure 32). These paths are not usually designed in; they just happen to be there. In fact, if D-type flip-flops are used, it is surprisingly difficult to get a "closed" set of illegal states (that is, a set such that once one of the illegal states is entered, the machine will forever remain in

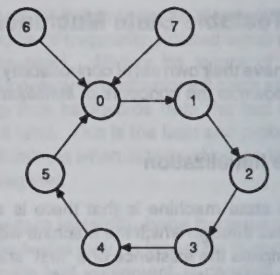


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Figure 31. Using Initialization to Recover

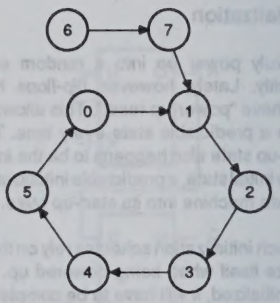

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Figure 32. Cycling Back to a Legal State

illegal states) by accident. In most cases, there will be a path which eventually leads back to a legal state. In these cases, merely clocking enough times will cause the machine to recover.

The drawback here is that one does not know ahead of time how many clock cycles will be needed. This necessitates some built-in way of knowing just when a legal state has been re-entered. And once that state has been reached, further cycling may be needed to get to a point where operation can resume.

Designing-in one-step recovery

The most predictable way of dealing with illegal states is to provide a one-step path back to a legal state. Depending on the state desired, more or less work may be involved to do this. For PAL devices, we can consider three cases:

- all illegal states go to state 00...0
- all illegal states go to one state other than 00...0
- each illegal state goes to some legal state

The cause of poor illegal state recovery can be illustrated conceptually with Karnaugh maps (although realistically, Karnaugh maps are often not used). When calculating the equations for a particular bit, it is tempting to use Don't Care cells from the Karnaugh map (Figure 33) to simplify the logic. The success of illegal state recovery depends on how these Don't Care cells are treated.

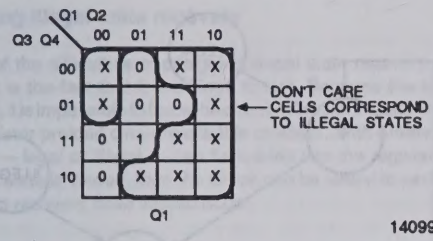
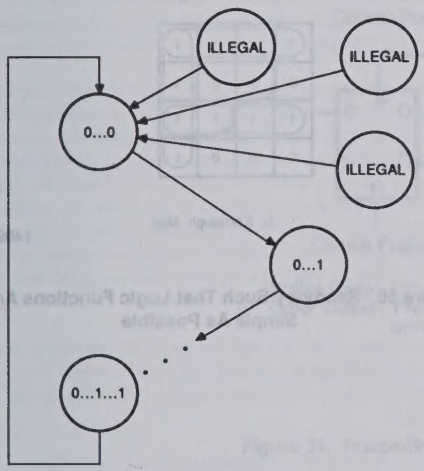


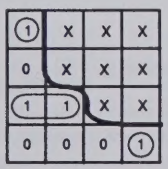
Figure 33. Illegal State

Recovering into state 00...0

This is the simplest case; it is illustrated in Figure 34. It is accomplished by not using any illegal states to generate the logic for any of the bits. Since most PAL devices have only D-type flip-flops, a bit will go HIGH only as a result of legal states. Any illegal states will cause all bits to be LOW.



a. State Diagram



b. Karnaugh Map

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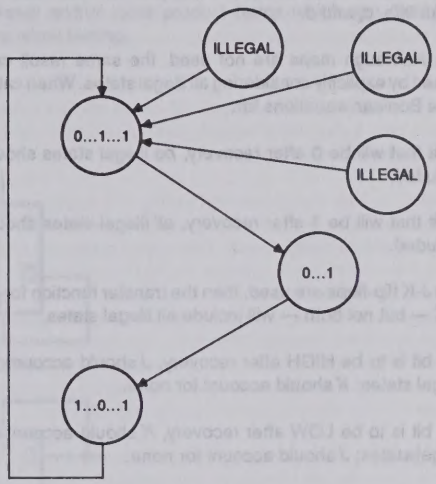
Figure 34. Recovering to State 0...0

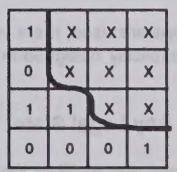
This procedure does not work when J-K or T-type flip-flops are used. In fact, it is deadly. Whereas a D-type flip-flop defaults to LOW, J-K and T-type flip-flops hold their present state as a default. Thus if illegal states are not considered in the transfer functions, an illegal state will cause the state machine to be locked up in that state.

Recovering into one fixed state

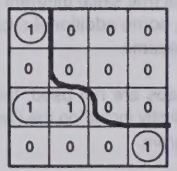
This case is shown in Figure 35a. The procedure can be illustrated conceptually with a Karnaugh map. It must first be decided which legal state will be entered, and the resultant value of each



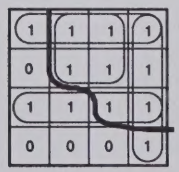
a. State Diagram



b. Karnaugh Map for Bit On



c. Bit On Recovers to 0



d. Bit On Recovers to 1

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Figure 35. Recovering to a State Other Than 0...0

state bit. The Don't Care cells for each bit are then filled with the corresponding next state bit value; if the next state for a bit is to be 1, then Don't Care cells are filled with 1's for that bit's Karnaugh map; the procedure for a 0-bit is analogous. The equations are now taken by including either all Don't Care cells if filled with 1's, or none of them if filled with 0's. This procedure is illustrated in Figures 35b, c, and d.

When Karnaugh maps are not used, the same result can be obtained by explicitly considering all illegal states. When calculating the Boolean equations for:

- a bit that will be 0 after recovery, *no* illegal states should be included.
- a bit that will be 1 after recovery, *all* illegal states should be included.

When J-K flip-flops are used, then the transfer function for either J or K — but not both — will include all illegal states.

- If a bit is to be HIGH after recovery, *J* should account for all illegal states; *K* should account for none.
- If a bit is to be LOW after recovery, *K* should account for all illegal states; *J* should account for none.

This must be done explicitly for J-K flip-flops even if state 0...0 is the recovery state.

When T-type flip-flops are used, there is no easy way out; any recovery must be explicitly designed-in as part of the original function.

Recovering Into Any Legal State

The third case allows one to fill in the Don't Care cells of a Karnaugh map in such a way that some legal next state is always reached in one clock cycle, but such that the 1's and 0's are placed to keep the logic functions simple. This is shown in Figure 36. The disadvantage here is that since different illegal states result in a different legal state, some additional cycling may be required to allow operation to resume.

When Karnaugh maps are not used, this can be implemented more simply by explicitly including the illegal states as part of the complete state diagram.

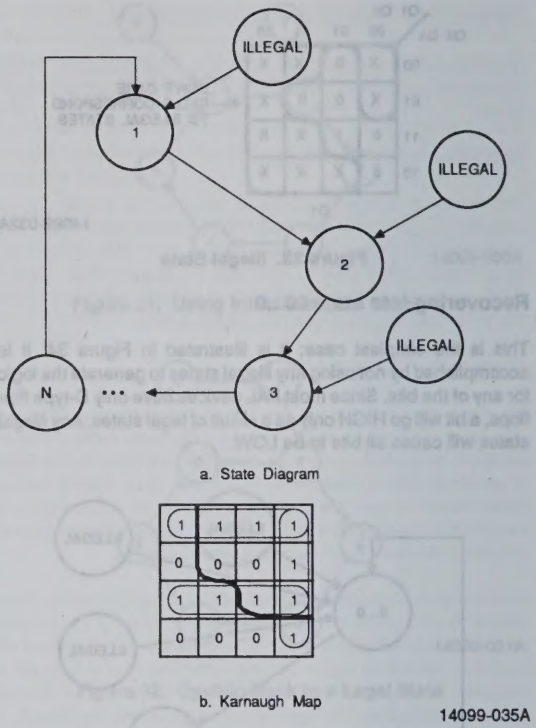
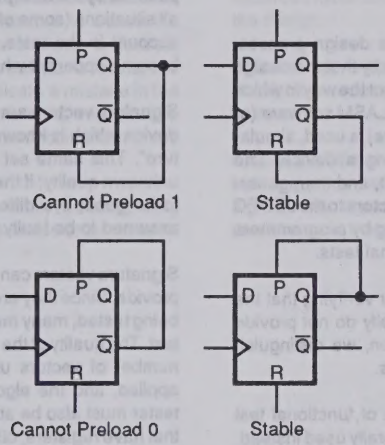


Figure 36. Recovery Such That Logic Functions Are As Simple As Possible

Testing illegal state recovery

One of the difficulties of designing illegal state recovery into a circuit is the fact that it is difficult to test. Because the state is illegal, it is impossible to force the circuit into such a state. The use of register preload circumvents this problem. With preload, any state — legal or illegal — can be loaded into the register. If an illegal state is loaded, then the circuit can be tested to verify that correct recovery does indeed occur.

The use of preload must be considered carefully with devices having programmable asynchronous preset and reset features. If these are driven by feedback from an output, then situations can occur where preloading one state immediately causes a preset or reset to the opposite state (Figure 37). There are two alternatives: either avoid preloading such states, or include a control input in the preset and/or reset product terms which can disable the feature when testing.



Stable Case: Can preload any state
Other Cases: Preloading any state will cause PRESET or RESET to opposite state.

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Figure 37. Preloading Registers with PRESET and RESET

Using Test Vectors

Digital systems are generally tested by applying a sequence of test vectors. A test vector is a group of signals which are applied (forced) and measured (sensed) on a device or a board. The vector thus defines all inputs and expected outputs for a given test. As we have noted, the sequence of tests performed greatly affects the quality of the overall tests, as measured by the fault coverage.

In general, we can talk in terms of three kinds of vectors. *Simulation* (or application) vectors, *functional* test vectors and *signature* test vectors.

Simulation vectors are generated during the design process. Their main purpose is to help the designer verify that the design has been correctly implemented. They represent the way in which the circuit was intended to operate. When PALASM software (or almost any other PLD design software package) is used, simulation may be performed prior to programming a device. The software simulates the operation of the circuit, and then generates vectors from the simulation, adding the vectors to the JEDEC file. These vectors can then be used for testing by programmers that have the capability of performing functional tests.

While simulation vectors may be adequate for verifying that the design is operating as expected, they generally do not provide very extensive test coverage. For this reason, we distinguish functional test vectors from simulation vectors.

It is very difficult to generate a complete set of functional test vectors by hand; computer programs are generally used instead. The simulation vectors are often used as a basis for generating a more comprehensive set of functional test vectors; in this capacity, the simulation vectors serve as *seed* vectors. There are many programs which perform this function although many of the programs require larger computers and take a long time to run. AMD also generates functional test vectors for patterns that are used in ProPAL devices.

Programs have been developed to generate vectors for use in testing PLDs. These programs use the programming information in the JEDEC file to generate tests.

On most patterns, they can generate test sequences of high quality. If complex internal feedback is used in a particular design, then some manual test generation may still be needed to improve the test coverage. Both of these programs support the use of register preload for initializing states.

While functional vectors provide more extensive tests, they may not exercise the circuit in the manner in which it was meant to be used. Thus, for example, a conditional oscillator in a circuit (as discussed previously) may not be a problem during simulation, since the conditions causing oscillation are not thought to be possible by the designer. However, the functional vectors will take all situations (some of which may not be physically possible) into account in the tests. Thus more subtle design problems may become apparent when functional test vectors are generated.

Signature vectors are random vectors which are first applied to a device which is known to be good in order to generate a "signature". This same set of vectors is then applied to a device of unknown quality; if the same signature results, the device is said to be good; if a different signature results, then the device is assumed to be faulty.

Signature vectors can vary greatly in the quality of testing they can provide. Since they are generated with no knowledge of the circuit being tested, many more vectors must be used to perform a good test. The quality of the test depends on the circuit being tested, the number of vectors used, the speed with which the tests are applied, and the algorithm used to generate the vectors. The tester must also be able to apply a preload sequence to devices that have registers; otherwise two devices may power up into two different states. In that case, both devices will generate different signatures even if both are good devices.

Quality signature testing can be very cost effective, since no advance knowledge of a device pattern is needed. This reduces the amount of resources that must be dedicated to test vector generation.

The different types of vectors are summarized in Table 1 below.

TYPE OF VECTOR	PURPOSE	GENERATED BY:
Simulation (Application)	Used for verifying whether or not a design will operate as expected when implemented.	Sequence defined by the design engineer, usually by hand. Actual vectors generated by design software, placed in the JEDEC file.
Functional	Used for verifying that a device is operating correctly.	Usually generated by a computer program. The simulation vectors can be used as seed vectors
Signature	Used for verifying that a device is operating correctly without functional vectors.	The tester generates the test sequence during the test.

Table 1. Test vectors

SUMMARY

The time to start considering ways of testing a circuit is before the circuit has been designed. The key to testability lies in the way the circuit is implemented.

Basic combinatorial logic can be made completely testable simply by minimizing logic. It is not even necessary to analyze the circuit for redundancy or reconvergent fanout; automatically minimizing all logic will eliminate any occurrences.

Where a sequential circuit is generated from simple feedback paths in the logic, the circuit must be analyzed as a combinatorial circuit. All combinatorial logic must be included to determine whether the circuit is a latch or an oscillator. If a latch is desired, it should be completely controllable. If an oscillator is found, it is probably not desired, and will generally indicate a mistake in the design. If a conditional oscillator is to be tolerated, one must be sure that the oscillation conditions can never occur, and that the test procedure will not cause oscillation.

In general, combinatorial circuits should be analyzed completely for the presence of latches and oscillators (wanted or unwanted). This can be done by simplifying each combinatorial logic block to see whether any signal ultimately depends on itself.

When the sequential nature of a circuit is derived through the use of flip-flops to generate a state machine, the two key issues are initialization and illegal state recovery. A combination of device features and careful circuit design will yield circuits that can behave predictably even in unexpected situations.

It is important to analyze the testability of a circuit before committing it too far. Thus any changes can be made early on. In particular, if the test analysis software points out any logic hazards in your circuit, you can easily remedy them by modifying the design.

These simple steps, taken early in the design phase, can help avoid later redesigns, and ultimately provide a higher quality system.

Finally, the ultimate test quality depends also on the quality of the test sequence used for production, functional test vectors and high quality signature tests will provide you with the highest confidence in the quality of your system.

Terminating High-Speed PAL Devices

INTRODUCTION

As system speeds have increased, designers have been requesting increasingly higher performance from their PAL devices. In the past, it has been possible for manufacturers to increase the device speed merely by reducing the internal delays of the part. Now, however, it has become impossible to design a 7.5-ns device with 4- or 5-ns rise and fall times, so the rise and fall times have been decreased to help speed up the devices.

Once the rise and fall times of a signal have dropped to a time that approximates the actual propagation delay of the signal on the wire, the realm of transmission lines has been entered. When this happens, the signal may become distorted due to reflections on the line. If severe enough, these reflections can cause such problems as gross overshoot and undershoot, extended ringing, crosstalk, and increased high-frequency emissions.

The reflections are caused by discontinuities in the impedance of the signal path, otherwise known as "impedance mismatches." In digital circuits, these usually occur at the end of the line; therefore, this becomes an issue of terminating the signals correctly. This application note will describe termination fundamentals, and compare the two basic termination schemes: serial termination and parallel termination.

Transmission Line Model

A transmission line can be represented by a lumped constant RLC circuit of unit length, as shown in Figure 1.

When dealing with digital circuitry on a pc board, both the resistive and conductive components are usually insignificant, and are ignored during transmission-line calculations. Called a lossless and loadless transmission line, this model can be represented by the following differential equation:

$$\frac{d^2}{dx^2} v = L_0 C_0 \frac{d^2}{dt^2} \qquad (1)$$

where: v = velocity

x = displacement along the line

t = time

L_0 = inductance per unit length of the transmission line

C_0 = capacitance per unit length of the transmission line.

Using convolution and Fourier analysis, the solution of this differential equation is as follows:

$$v = \frac{1}{\sqrt{L_0 C_0}} . \qquad (2)$$

The propagation delay, t_{PD}, of a unit length is therefore expressed as

$$t_{PD} = \sqrt{L_0 C_0} . \qquad (3)$$

The inductance and capacitance in the presence of a ground plane are a function of the dielectric medium and pc-board layout. Unit values of the inductance and capacitance can be measured by an LC meter. In general, transmission line effects can be simulated in both time and frequency domains with the SPICE circuit-analysis program.

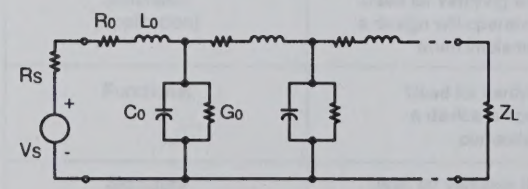

Figure 1. Equivalent Circuit of a Transmission Line

Transmission Line Geometries

Circuit interconnections for high-speed digital systems generally include the following types:

- connectors
- wire over a ground plane
- twisted pair
- coaxial cable
- microstrip line
- strip line

Connectors generally cause wave-shape distortion when transition times are under 1 ns. The transmission-line effects of wire over a ground plane are uncontrollable; this type of interconnection is usually used for

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prototypes only. Twisted pair and coaxial cable are generally reserved for applications such as differential lines and video cable. The remaining two types of interconnections, microstrip and strip line, are the most practical for high-speed digital systems and will be discussed here in detail.

A microstrip line (Figure 2a) is a metal-strip conductor on the pc board, separated from a conducting plane with a dielectric medium. The characteristic impedance Z_0, which is the ratio of voltage to current for a traveling wave at any given point and instant, is

$$Z_0 = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98\,d}{0.8\,w + t}\right), \quad (4)$$

where e_r is the dielectric constant of the board material. This equation is fairly accurate for a w/d ratio between 0.1 and 3.0 and for e_r between 1 and 15. For G-10 fiber-glass epoxy boards, e_r is about 5.0.

The equations for inductance per foot, L_0, and propagation delay per foot of the line, t_{PD}, are

$$L_0 = Z_0^2\, C_0 \quad \text{and} \quad (5)$$

$$t_{PD} = 1.017\sqrt{0.475\,e_r + 0.67} \ \text{ns/ft}, \quad (6)$$

where C_0 is capacitance per foot.

A strip line (Figure 2b) is a metal-strip conductor centered in a dielectric medium between two conducting planes. The characteristic impedance, Z_0, is

$$Z_0 = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.67\,\pi\,w\,(0.8 + \frac{t}{w})}\right). \quad (7)$$

This equation is fairly accurate for

$$\frac{w}{b-t} < 0.35 \quad (8) \quad \text{and} \quad \frac{t}{b} < 0.25. \quad (9)$$

The equations for inductance per foot and propagation delay per foot of the line are

$$L_0 = Z_0^2\, C_0 \quad \text{and} \quad (10)$$

$$t_{PD} = 1.02\sqrt{e_r} \quad (11)$$

The characteristic impedance of both microstrip and strip lines can be held within 5% if all the variables (e_r, w, d, t) are controlled. Also, note that the propagation delay of both microstrip and strip lines is not a function of the pc board geometry, but of the dielectric constant only.

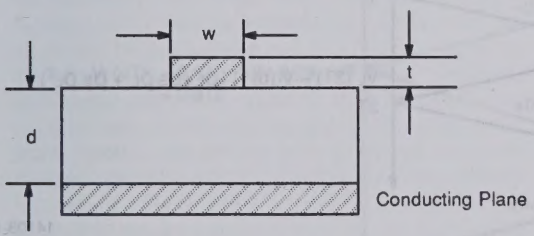

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Figure 2a. Cross Section for Microstrip Line

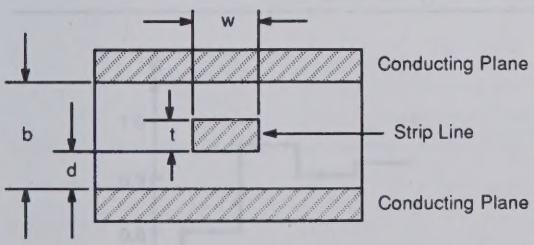

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Figure 2b. Cross Section for Strip Line

Reflections on the Transmission Line

Reflections on the transmission line are caused by a discontinuity of the line impedances, and are a major source of noise in digital systems. The discontinuity can appear as an input device, another circuit, a connector, or another transmission line.

Figure 3 shows the signal reflection and flow-through at the impedance discontinuity between transmission lines TL1 and TL2. The voltage reflection at the point of discontinuity travels back through TL1 with a magnitude of ρV_i, where ρ is the reflection coefficient and V_i is the incident-wave voltage.

The reflection coefficient is the ratio of voltage in the reflected wave to that in the incident wave as follows:

$$\rho = \frac{V_r}{V_i}. \quad (12)$$

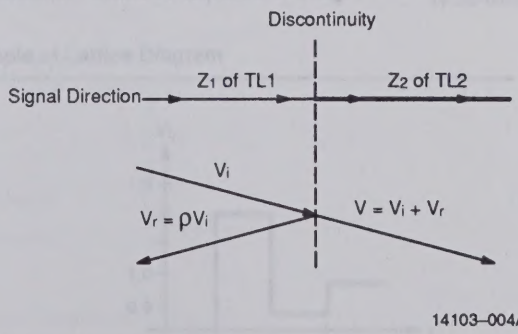

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Figure 3. Signal Reflection at a Discontinuity

The signal flow-through is $V_i + V_r$, where V_r is the reflected-wave voltage. From

$$V_r + V_i = V \quad (13)$$

and

$$\frac{V_r}{Z_1} - \frac{V_i}{Z_1} = \frac{V}{Z_2}, \quad (14)$$

we obtain

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1}, \quad (15)$$

where Z_1 and Z_2 are the characteristic impedances of transmission lines TL1 and TL2 respectively.

Figure 4 is an example of a basic transmission line with a discontinuity at both the source and load. In this basic reflection mode, fanout is one. A lattice diagram is widely used to illustrate the reflection effect on a transmission line. Two vertical axes, for the source and load, are the time scales. The signal bouncing back and forth along the transmission line is shown as a diagonal line from top to bottom.

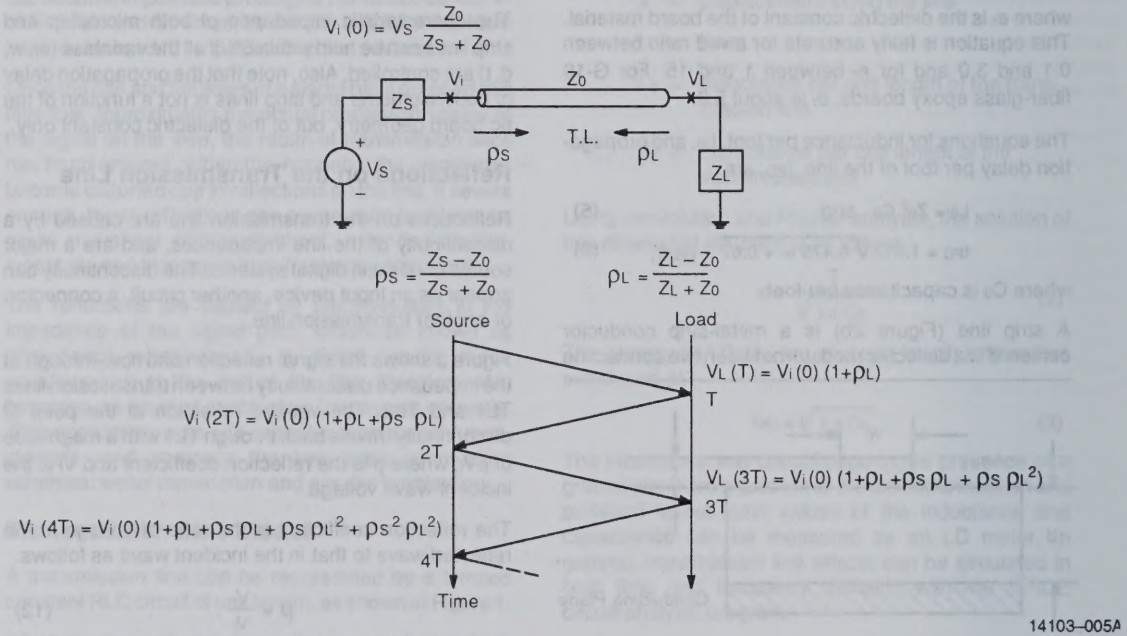

Figure 4. Example of Basic Transmission Line Circuit and its Lattice Diagram

The voltage V_i is the result of a voltage division between the source impedance Z_S and the line impedance Z_0. The voltage at each time interval is the algebraic sum of the reflection voltages from the top to the specific diagonal line. For example, the voltage at 4T is

$$V_i(0)(1 + \rho_L + \rho_L\rho_S + \rho_L^2\rho_S + \rho_L^2\rho_S^2), \quad \textbf{(16)}$$

where: ρ_S is the reflection coefficient at the source,

and ρ_L is the reflection coefficient at the load.

Figure 5a is a numerical example of the lattice diagram; note that V_i and V_L eventually reach the same steady-state voltage, as shown in Figures 5b and 5c.

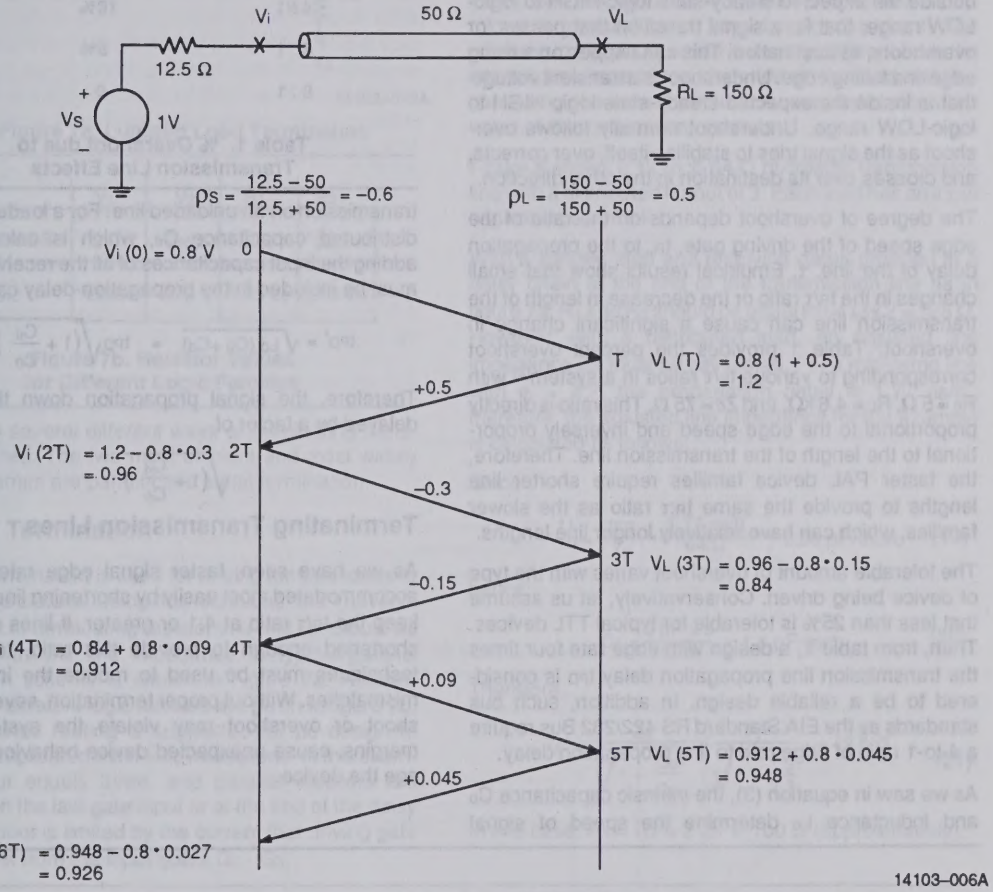

Figure 5a. Numerical Example of Lattice Diagram

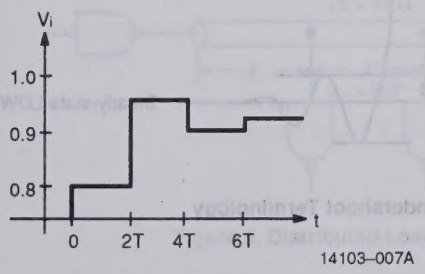

Figure 5b. Voltage at V_i

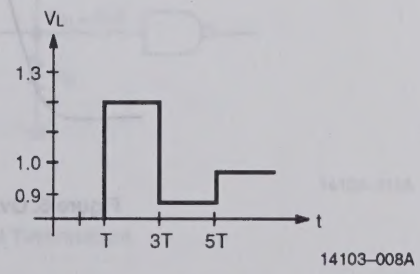

Figure 5c. Voltage at V_L

Only the transmission line effects that cause severe overshoot or undershoot need to be addressed. The rest, as long as they do not degrade the signal or interfere with data transmission, can be ignored.

The terms "overshoot" and "undershoot" are often used in different ways by different people. For this discussion, overshoot is defined as a transient voltage that is outside the expected steady-state logic-HIGH to logic-LOW range; that is, a signal transition that passes, or overshoots, its destination. This can happen on a rising edge or a falling edge. Undershoot is a transient voltage that is inside the expected steady-state logic-HIGH to logic-LOW range. Undershoot normally follows overshoot as the signal tries to stabilize itself, over corrects, and crosses over its destination in the other direction.

The degree of overshoot depends on the ratio of the edge speed of the driving gate, t_R, to the propagation delay of the line, τ. Empirical results show that small changes in the t_R/τ ratio or the decrease in length of the transmission line can cause a significant change in overshoot. Table 1 provides the percent overshoot corresponding to various t_R/τ ratios in a system[2] with $R_0 = 5\,\Omega$, $R_L = 4.6\,k\Omega$, and $Z_0 = 75\,\Omega$. This ratio is directly proportional to the edge speed and inversely proportional to the length of the transmission line. Therefore, the faster PAL device families require shorter line lengths to provide the same $t_R{:}\tau$ ratio as the slower families, which can have relatively longer line lengths.

The tolerable amount of overshoot varies with the type of device being driven. Conservatively, let us assume that less than 25% is tolerable for typical TTL devices. Then, from table 1, a design with edge rate four times the transmission line propagation delay t_{PD} is considered to be a reliable design. In addition, such bus standards as the EIA Standard RS 422/232 Bus require a 4-to-1 ratio of edge rate to line propagation delay.

As we saw in equation (3), the intrinsic capacitance C_0 and inductance L_0 determine the speed of signal transmission on an unloaded line. For a loaded line, the distributed capacitance C_d, which is calculated by adding the input capacitances of all the receiving gates, must be included in the propagation-delay calculation.

$t_R : \tau$	% overshoot at the end of loaded line
1 : 1	87%
2 : 1	63%
3 : 1	30%
4 : 1	10%
6 : 1	5%
8 : 1	0

Table 1. % Overshoot due to Transmission Line Effects

$$t_{PD}' = \sqrt{L_0 (C_0 + C_d)} = t_{PD}\sqrt{\left(1 + \frac{C_d}{C_0}\right)} \quad \textbf{(17)}$$

Therefore, the signal propagation down the line is delayed by a factor of

$$\sqrt{\left(1 + \frac{C_d}{C_0}\right)}. \quad \textbf{(18)}$$

Terminating Transmission Lines

As we have seen, faster signal edge rates can be accommodated most easily by shortening line length to keep the t_R/τ ratio at 4:1 or greater. If lines cannot be shortened enough to provide this ratio, termination techniques must be used to reduce the impedance mismatches. Without proper termination, severe undershoot or overshoot may violate the system noise margins, cause unexpected device behavior, or damage the device.

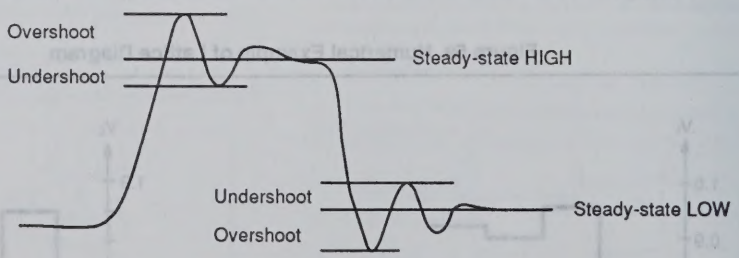

Figure 6. Overshoot and Undershoot Terminology

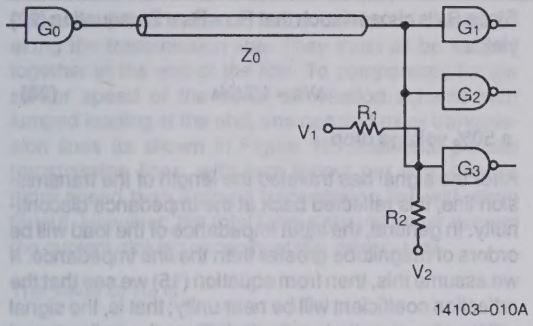

Figure 7a. Lumped Load Termination

	V_1	V_2	R_1	R_2
TTL, CMOS	5 V	GND	$2Z_0$	$2Z_0$
ECL	GND	–5.2 V	1.63 Z_0	2.60 Z_0

Figure 7b. Resistor Values for Different Logic Families

There are several different ways of terminating transmission lines. The two most efficient and most widely used schemes are parallel and serial termination.

Parallel Termination

Parallel termination is used for driving lumped loads or high-speed circuits. Using this technique, the Thevenin equivalent of terminating resistors R_1 and R_2 should be the same as the line impedance. A typical parallel termination scheme is shown in Figure 7a. Resistor values for different logic families are given in figure 7b. Daisy-chained routing is suggested for pc design to reduce complicated multi-level reflections. In this example, fanout equals three, and parallel resistors are inserted on the last gate input or at the end of the daisy chain. Fanout is limited by the current that driving gate G_0 can sink from the input gates G_1 - G_3.

The parallel-termination technique in figure 7a uses dual resistors and a single power supply. It is possible to use a single resistor with a Thevenin equivalent of the two resistors. This would require a second power supply which is usually not available, and therefore would be costly.

Parallel termination is also used for driving distributed loads, but the termination resistor values are determined by calculating an impedance adjustment. The adjusted impedance, which is usually different from the intrinsic line impedance, depends on the load distribution along the transmission line, and determines the value of the termination resistors.

Figure 8 shows a 12-inch 64-Ω microstrip transmission line with a distributed fanout of 3. Each load has an input capacitance of 6 pF.

With a lumped load and receiving gates grouped in a daisy chain at the end of the transmission line as in figure 7a, R_1 and R_2 should be equal to 64 Ω x 2 = 128 Ω. However, with a distributed load, an adjusted line impedance Z_0' must be calculated. For a microstrip line with e_r = 4.7, the propagation delay is 1.77 ns/ft.; therefore, the adjusted line impedance for the example is calculated as follows.

Since

$$C_0 = \frac{t_{PD}}{Z_0} = \frac{1.77\ \text{ns/ft}}{64\ \Omega} = 2.30\ \text{pF/inch}, \quad \textbf{(19)}$$

hence,

$$C_d = \frac{6\ \text{pF} \times 3}{12\ \text{in}} = 1.5\ \text{pF/inch}. \quad \textbf{(20)}$$

Therefore,

$$Z_0' = \frac{Z_0}{\sqrt{1 + \frac{C_d}{C_0}}} = \frac{64\ \Omega}{\sqrt{1 + \frac{1.5}{2.3}}} = 49.8\ \Omega. \quad \textbf{(21)}$$

In this case, $R_1 = R_2 = 2\ Z_0' = 100\ \Omega$ (approximately).

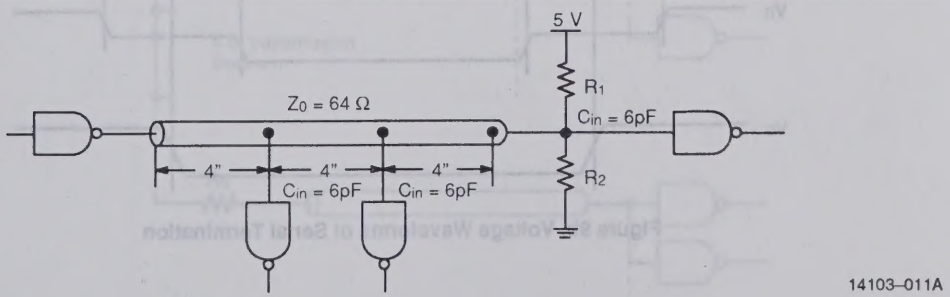

Figure 8. Distributed Loads with Parallel Termination

Serial Termination

A series resistor Rs is useful for dampening overshoot and ringing on longer lines. With serial termination, Rs plus the gate output impedance Ro should be equal to the line impedance Z_0. Since this technique is quite straightforward and applicable to all logic families, most interconnections with uncontrollable line impedance (lines in conjunction with connectors, a circuit board layout without a ground plane, wire-wrapped connections, or lines associated with back plane) use this scheme.

Serially-terminated lines display characteristic AC behavior as the signal switches. Figure 9a shows a simple circuit with a driving gate G_0 connected to gate G_1 with a fanout of 1, via a transmission line with line impedance Z_0. Presumably, as voltage V_A changes from HIGH to LOW at time t_1 (see figure 9b), V_B changes simultaneously, as follows:

$$\Delta V_B = \Delta V_A \frac{Z_0}{R_O + R_S + Z_0} . \qquad (22)$$

Since Rs is chosen such that $R_O + R_S = Z_0$, equation (22) yields

$$\Delta V_B = 1/2 \Delta V_A , \qquad (23)$$

a 50% voltage drop.

After the signal has traveled the length of the transmission line, it is reflected back at the impedance discontinuity. In general, the input impedance of the load will be orders of magnitude greater than the line impedance. If we assume this, then from equation (15) we see that the reflection coefficient will be near unity; that is, the signal will be almost entirely reflected. Thus the indicent and reflected waves will combine to provide a low voltage at point C.

As the reflected wave travels back up the transmission line, it eventually brings point B LOW. Since $R_O = R_S$, there is no impedance mismatch at the source, and the reflection is absorbed. This is confirmed by equation (15), which shows that the reflection coefficient is 0 at the source.

The reverse process occurs when the signal changes from LOW to HIGH, as shown in Figure 9b.

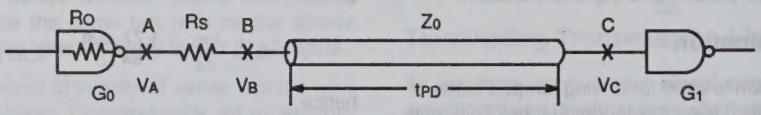

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Figure 9a. Example of Serial Termination

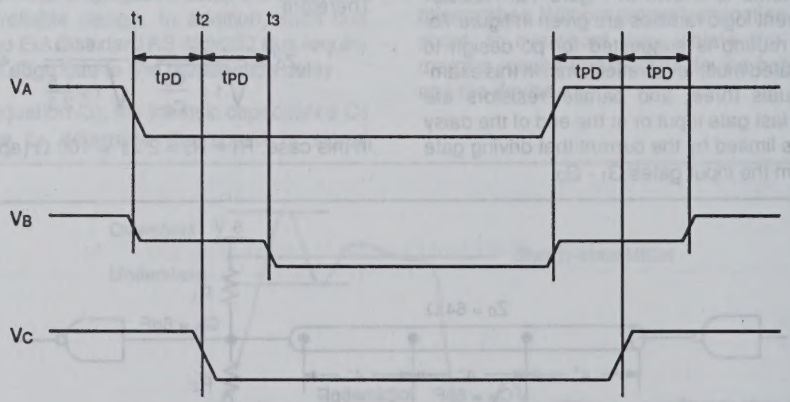

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Figure 9b. Voltage Waveforms of Serial Termination

Because of this behavior, loads cannot be distributed along the transmission line. They must all be lumped together at the end of the line. To compensate for the slower speed of the serial termination scheme with lumped loading at the end, one can add more transmission lines as shown in Figure 10. Additional parallel transmission lines, with less fanout per line, provide more speed than a single transmission line with more fanout. However, the total fanout should never exceed the current-sinking capacity of the driving gate.

The value of Rs is

$$Rs = Z_0 - nR_0 , \quad (24)$$

where n is the number of parallel transmission lines. Note that this equation limits the number of parallel lines possible, since Rs will be negative if n is too large.

Comparison Between Parallel and Serial Termination Schemes

- Serial termination consumes less power than the single-power-supply parallel termination technique across the entire frequency spectrum. This is primarily because series termination does not add a DC load to the drivers.
- Parallel termination requires two resistors or one resistor with two power supplies. Serial termination requires one resistor per transmission line.
- With series termination, distributed loading cannot be used along the line because of the 50% voltage drop discussed above. With parallel termination, the waveform is undistorted along the entire transmission line, so that the loads can be distributed anywhere along the line as long as the terminating resistor values are adjusted. In either case, fanout is limited by the current-driving capability of the driving gate.
- If a long line is required or if power consumption is a concern, serial termination can be more advantageous. When speed is a main factor, parallel termination is better. Loading a long transmission line does not increase the t_{PD} of the driving gate nor its edge rate. However, it does increase the line capacitance, and consequently the line propagation delay. It has been proven[1] that delay time with loading increases twice as much with series termination as with parallel termination.

Board Layout Techniques for Transmission Lines

Once the type of transmission line is determined, board layout becomes critical. The following guidelines will help keep signals clean.

- Keep signal interconnections as short as possible to increase the t_R/τ ratio.
- Provide a separate signal plane; at least one ground plane and one power plane are recommended.
- Include a 0.1-μF decoupling capacitor as close as possible to the ground plane and the V_{CC} pin on each high-speed logic device.
- Provide both 0.1-μF ceramic high-frequency and 100-μF electrolytic low-frequency filtering capacitors on the power inputs to the board.
- Use wide line spacing between high-speed lines to avoid crosstalk.

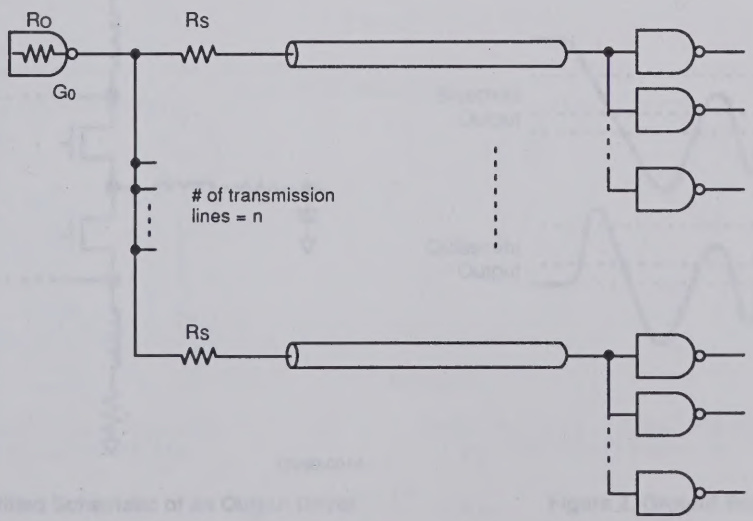

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Figure 10. Serial Termination with Multiple Transmission Lines

- Do not exceed maximum AC loading specifications, which include capacitive and current loading.
- Avoid anything that might cause an impedance mismatch on the line, such as sharp corners or discontinuities on the conducting plane.
- Such critical lines as edge-triggered signals or high-current driving signals should be separated from ordinary level-sensitive signals. In addition, sensitive circuitry, such as a clock oscillator, should have a separate ground to minimize noise interference.

CONCLUSION

As logic speed increases, edge rates becomes sharper; however, transmission line speeds remain the same if loading is not changed. Therefore, to avoid increased ringing, the maximum line length must shrink. As a result, if a line longer than the maximum permissible line length is required, proper termination must be provided. These careful design practices will ensure that your signals are clean, providing your system with better performance and reliability.

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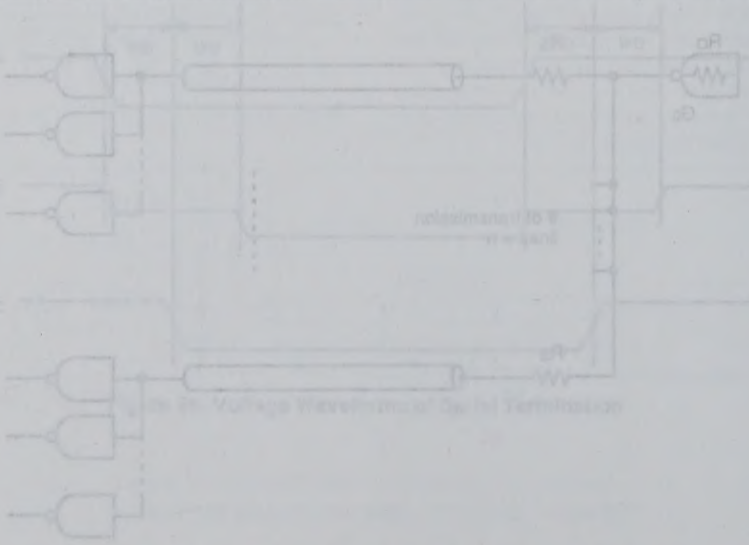
(1) William R. Blood, Jr. "ECL Systems Design Handbook," Motorola Semiconductor Products Inc., Mesa, AZ, May, 1983 (fourth edition); Chapters 3 and 7.

(2) K. M. True, "Reflections: Computations and Waveforms," The Interface Handbook, Fairchild Corp., Mountain View, CA, 1975, Chapter 3.

(3) Ramo, Whinnery, and Van Duzer, "Fields and Waves in Communication Electronics," John Wiley & Sons, 1965, Chapter 1.



Ground Bounce

INTRODUCTION

The development of fast PAL devices has increased the importance of analog considerations the digital designer has been able to overlook in the past. One of these is ground bounce. Ground bounce refers to the ringing on an output signal when one or more outputs on the same device are being switched from HIGH to LOW. This ringing can be in excess of 3 V. The system cannot consider the data valid until the ringing settles to below the V_{IL} of the receiving devices. The ringing in a fast device can last so long that a slower device with less ground bounce could actually be a faster solution.

The phenomenon of ground bounce is associated with the inductance and resistance of the ground connection in the integrated circuit. As there is always some inductance and resistance, ground bounce cannot be totally eliminated; however, it can be reduced to a level tolerable to the system.

This article will discuss the mechanism of ground bounce in CMOS circuitry and the utilization of slew-rate control used by AMD to keep ground bounce down to reasonable limits.

Mechanism

Figure 1 shows a schematic of an output driver and load including parasitic elements. The load capacitor is charged to the HIGH-level voltage. When the transistor turns on, the capacitor discharges into the transistor and lead impedance. The resultant RLC circuit will have a damped ringing (Figure 2). The peak amplitude depends on the edge rate of the switch and the RLC values, while the frequency of the ringing and the rate of decay depend only on the RLC values.

The ringing caused by a single output switching is normally below the LOW-threshold voltage. However, the voltage at the ground pad of the device is proportional to the number of outputs switching simultaneously. In addition, the voltage at the ground pad is coupled to any LOW output through its output transistor. Therefore, if enough outputs switch, ringing on the ground pad will be coupled to LOW outputs, causing the detection of false HIGHs.

Most PAL devices used today have relatively low output drive current: 16 mA or 24 mA. It is tempting to think that the low current level will somehow limit the switching en-

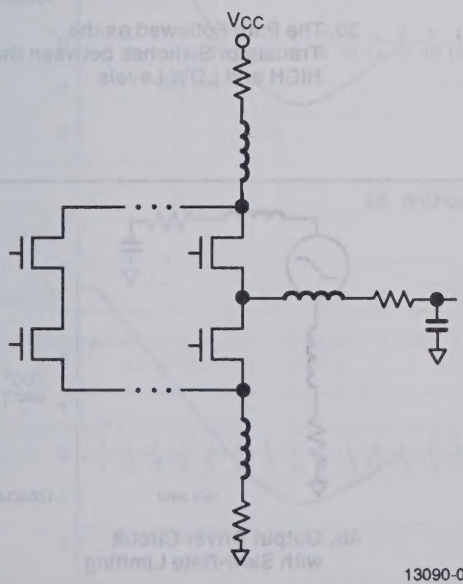


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Figure 1. Simplified Schematic of an Output Driver

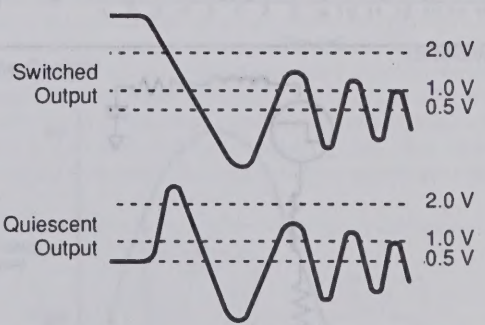

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Figure 2. Ground Bounce

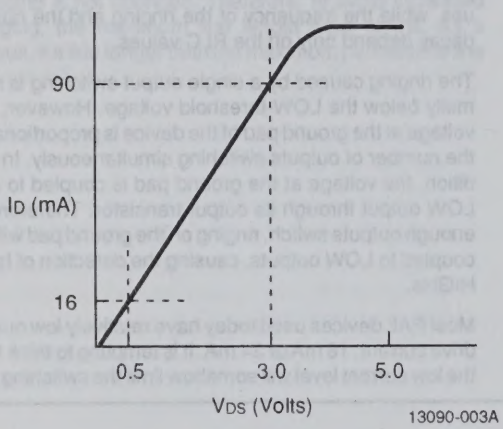
ergy and therefore ground bounce. Actually, even a low-power transistor can pass a relatively large current. The transistor I-V curve in Figure 3a shows that a MOS transistor designed for 16 mA at 0.5 V will pass 90 mA at 3.0 V. Figure 3b shows the V/I path when the output transistor switches between HIGH and LOW. Notice that the transistor switches from 3.5 V at 0 mA to 3.0 V at 90 mA. If eight outputs were to switch simultaneously, 90 mA X 8, or 720 mA, would flow through the ground lead.

This sudden current surge is actually self-limiting. As the ground-pad voltage rises due to the high current change, the internal V_{DS} and the available gate bias voltage are reduced, lowering the drive current. However, the ringing can still exceed 3 V.

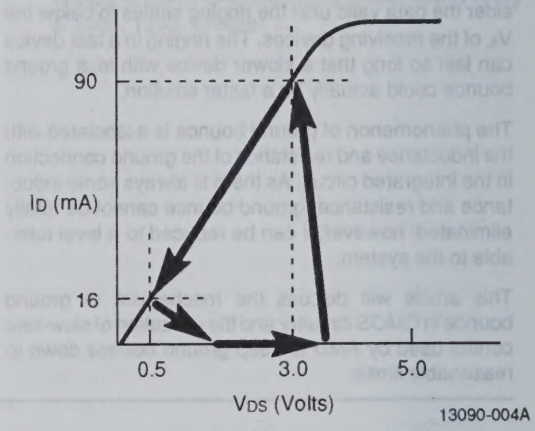
Controlled Edge Rate

The parameters that influence ground bounce are the inductances and resistances of the device, the capacitance of the load, and the edge rate. Of these, the only one that the chip manufacturer can directly control is the edge rate.

Turning on the output-driver transistor is equivalent to switching the charged load capacitor to ground. This can be represented by a step-voltage source in series with the capacitor (Figure 4a). Slowing down the rate that the output transistor can turn on changes the voltage source from a step to a ramp (Figure 4b). With a

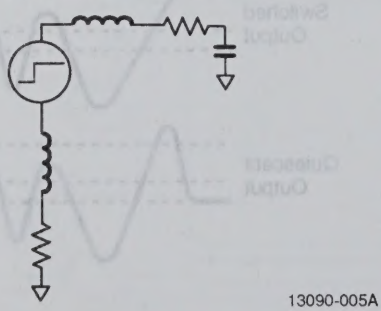


3a. The DC Curve of an Output Driver Transistor

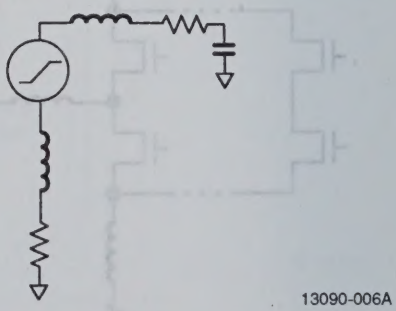


3b. The Path Followed as the Transistor Switches between the HIGH and LOW Levels

Figure 3.



4a. Equivalent Circuit of an Output Driver Transistor with a Capacitive Load



4b. Output Driver Circuit with Slew-Rate Limiting

Figure 4.

shallower slope, less energy is available for ringing and the ground-bounce amplitude is reduced.

A Spice simulation (Figure 5) illustrates the effect. The device without risetime control will have a very high charging current with a large di/dt: 2.1 X 10^7 A/s. Risetime control reduces the di/dt about 25%. This will result in a corresponding reduction in the voltage that can develop across the ground inductance.

AMD has a proprietary technique that slows the edge rate of the output transistor, thereby reducing the amplitude of the ringing. Slowing down the fall time will add about a nanosecond to the output delay, but the system speed will still be greatly increased. On a high-capacitance load, a non-edge-rate-controlled device could ring for more than 25 ns. The additional delay required to allow for the ringing would be intolerable.

System Ground Bounce Solutions

There are some things that the system designer can do to reduce the ground bounce to a tolerable level.

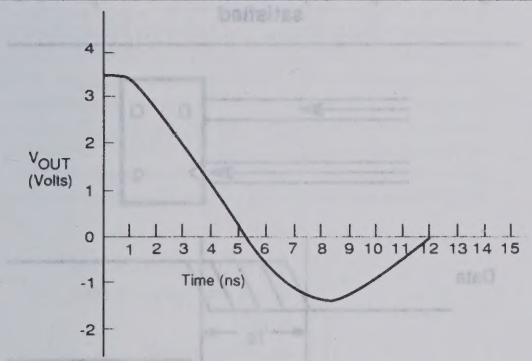
1) Use AMD PAL devices that incorporate edge rate control. This the first line of defense against ground-bounce-related problems, and the most effective.

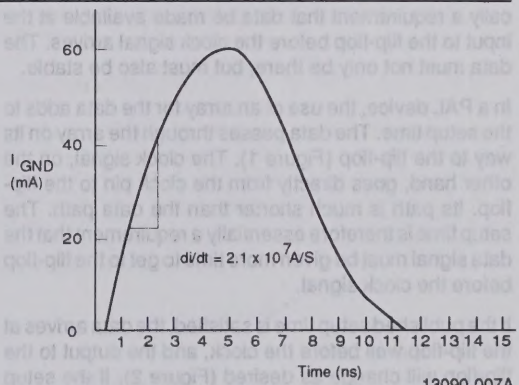
2) Use shorter lead packages. The bonding wires in a PLCC are 1/4 the length of the ground bonding wire in a DIP. The inductance is reduced proportionally. Any reduction in inductance will reduce the amplitude of the ringing.

Some devices have center power and ground pins. The ground pin will be substantially shorter and have a proportionately reduced inductance. This will reduce the coupling between outputs. A good example is the PALCE26V12.

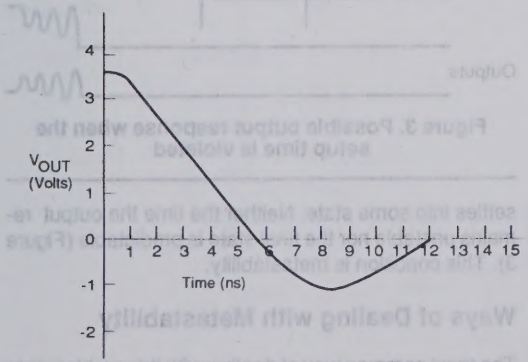
3) Reduce capacitive loading. Capacitive loading in any system should be reduced as much as possible. This may involve consideration of the transmission line characteristics of the layout.

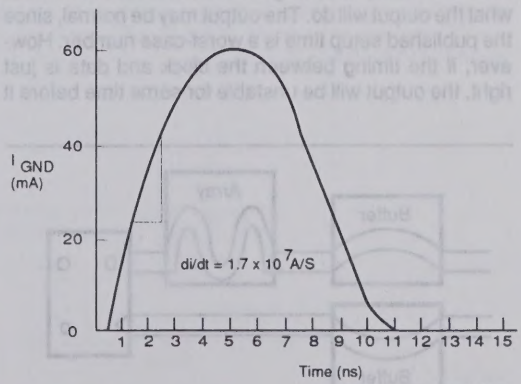
4) Limit the number of outputs switching simultaneously. If the load naturally has high-capacitance such as a bus or memory board would, ground bounce can be reduced by limiting the number of outputs that can switch simultaneously in a single device. Many system designers consider 4 to be an acceptable upper limit.





5a. Without Risetime Control





5b. With Risetime Control

Figure 5. Effect of Risetime Control

Metastability

INTRODUCTION

A significant number of digital systems must deal with inputs not synchronized to their own internal clocks. These asynchronous signals can arise from any of the various asynchronous protocols, such as are often used in bus designs; they can be the result of trying to share signals from systems with different clocks; or they may be the response of a system user, who is of course not synchronized with the system. The result can be metastability, a problem which can plague unwary designers. It is not a newly discovered phenomenon, but is normally dealt with somewhat qualitatively, and, unfortunately, is usually ignored as much as possible.

Causes of Metastability

The flip-flop setup time is the parameter that is most often at the root of metastability. The setup time is basically a requirement that data be made available at the input to the flip-flop before the clock signal arrives. The data must not only be there, but must also be stable.

In a PAL device, the use of an array for the data adds to the setup time. The data passes through the array on its way to the flip-flop (Figure 1). The clock signal, on the other hand, goes directly from the clock pin to the flip-flop. Its path is much shorter than the data path. The setup time is therefore essentially a requirement that the data signal must be given more time to get to the flip-flop before the clock signal.

If the published setup time is satisfied, the data arrives at the flip-flop well before the clock, and the output to the flip-flop will change as desired (Figure 2). If the setup time is violated, then no guarantee can be made about what the output will do. The output may be normal, since the published setup time is a worst-case number. However, if the timing between the clock and data is just right, the output will be unstable for some time before it settles into some state. Neither the time the output remains unstable nor the final state is predictable (Figure 3). This condition is metastability.

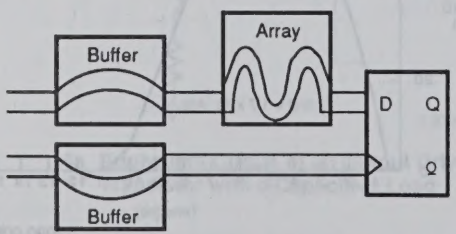


Figure 1. The clock and data paths in a PAL device

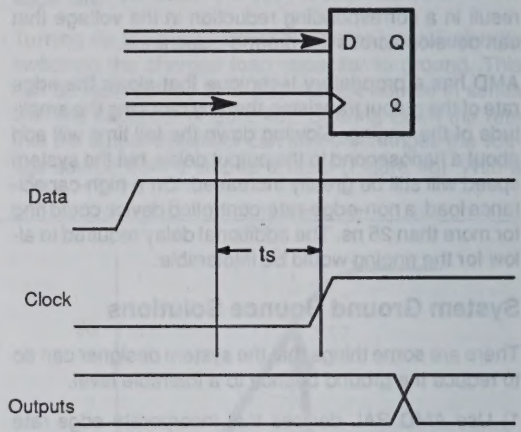


Figure 2. Output response when the setup time is satisfied

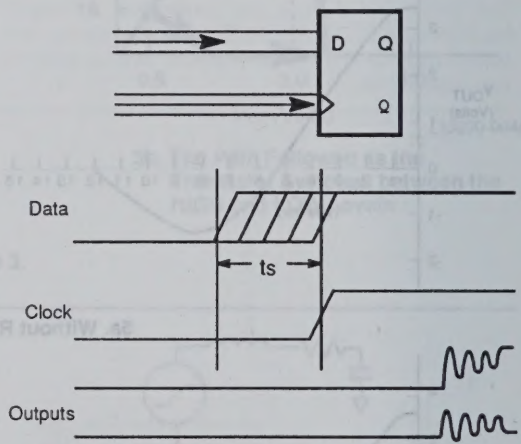


Figure 3. Possible output response when the setup time is violated

Ways of Dealing with Metastability

The most common way of dealing with this problem is to synchronize the inputs with an extra flip-flop (Figure 4). If the first flip-flop goes metastable, hopefully the delay between clock pulses will allow the ringing to die down

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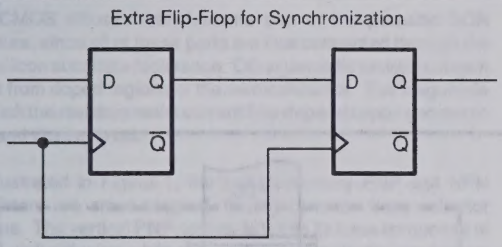

Figure 4. Dual synchronizer

before clocking into the next flip-flop. This improves the chances of having good data in the second flip-flop.

This method is not without its costs. Each extra stage of flip-flop means an extra clock delay of the data which must be absorbed by the system. Moreover it is not foolproof. The possibility of metastability is reduced, but not eliminated. A flip-flop can go metastable if the preceding stage does not recover quickly enough.

The best way to avoid metastability is to avoid synchronization when possible. Many applications, such as bus arbitration schemes, use synchronization not because synchronization itself is necessary, but because it provides the only convenient way to store data. This unfortunately takes a system that is inherently asynchronous and adds some synchronizing elements in the middle.

Summary

Metastability can occur in a number of different kinds of asynchronous systems, usually due to the inability to guarantee that the setup time of the flip-flops will be satisfied. In standard synchronous systems, where the setup time (along with all other timing requirements) is specifically designed in, metastability will never be a problem.

In some situations, metastability is caused by the need to interface systems with different clocks. In this case, it will never be possible to completely eliminate the possibility of metastability. Instead, the designer must take steps to reduce the probability of a system failure due to metastability.

Latchup Circuit

Latchup is caused by an SCR (Silicon Controlled Rectifier) circuit. Fabrication of CMOS integrated circuits with bulk silicon processing creates a parasitic SCR structure. The behavior of this SCR is similar in principle to a true SCR. These structures result from the multiple diffusions needed for the formation of complementary MOS transistors in CMOS processing. The SCR structure consists of a four layer device formed by diffused PNPN regions. These four layers create parasitic bipolar transistors illustrated in Figure 1.

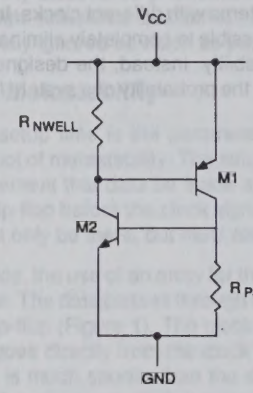

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Figure 1

Figure 2a shows a typical CMOS inverter layout with the schematic of the parasitic bipolar SCR structure. Figure 2b is a cross sectional representation of the CMOS inverter, again with the schematic of the bipolar SCR structure.

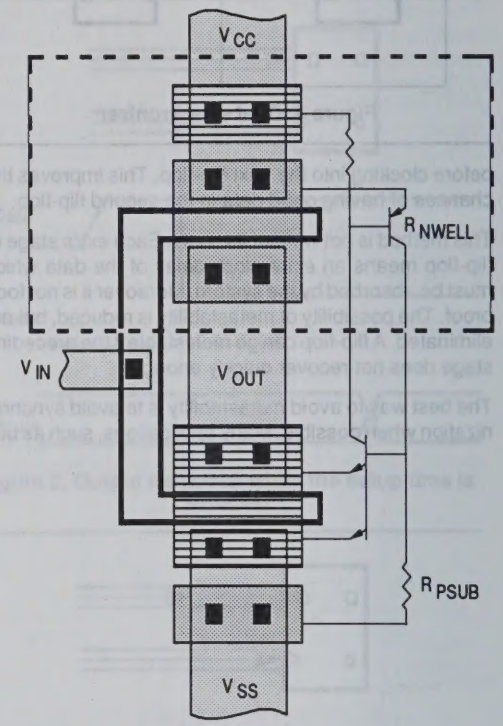

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Figure 2a

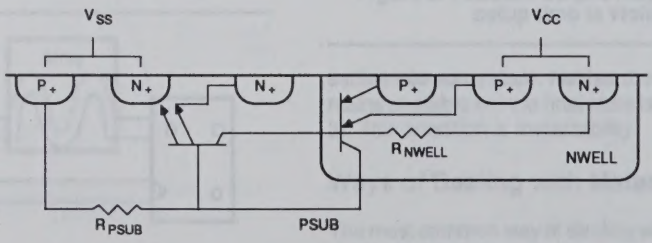

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Figure 2b

Any CMOS diffusion can become part of the parasitic SCR structure, since all of these parts are interconnected through the bulk silicon substrate resistance. Other parasitic resistors shown result from doped regions of the semiconductor. The magnitude to which the resistors resist current flow depends upon geometric size and doping level.

As illustrated in Figure 1, the complementary PNP and NPN transistors are cross-coupled, having common base-collector regions. The vertical PNP device, M1, has its base composed of the N-well diffusion while the emitter and collector are formed from P-type source-drain and substrate regions, respectively. The lateral bipolar transistor, M2, base is the P substrate with emitter and collector junctions formed from N-type source-drain and N-well diffusions, respectively.

Latchup Conditions

Under normal bias conditions the SCR conducts only leakage current and the SCR structure is in the blocking state. However, as current flows across any of the parasitic resistors, a voltage drop is developed, turning on the parasitic bipolar base-emitter junction. The forward bias condition of this junction allows collector current to flow in the bipolar transistor. This collector current flows across the base-emitter resistor of the complementary bipolar transistor, creating a voltage sufficient to turn on the transistor.

A regenerative loop is now created between the complementary bipolar transistors such that current conduction becomes self-sustaining. Even after removal of the stimulus that triggered this action, the current conduction can continue. This region of operation is a high-current, low-resistance condition characteristic of a four layer PNPN structure. This is referred to as latchup. Once initiated, the excessive latchup current can permanently damage an integrated circuit by fusing metal lines or destroying junctions.

Causes Of Latchup

Latchup may be initiated in numerous ways. Just the critical causes frequently encountered in a system environment will be discussed. These include power up, supply overvoltage, and overshoot/undershoot at device pins.

Power-Up

Caution must be exercised when powering up CMOS ICs to avoid driving device pins before the supply voltage has been applied to the circuit. Placing a device or board in a "hot socket" will create this situation. When subjected to hot socket insertion, voltage conditions at the device pins are uncertain such that the input diodes may be forward biased. Forward biasing the input diodes with a delayed or uncontrolled application of V_{CC} could cause the device to latch up. Advanced Micro Devices' CMOS circuits have substantial immunity to hot-socket power up, but since this condition is uncertain, and difficult to characterize, test, and guarantee, it should be avoided.

Supply Overvoltage

Supply levels exceeding the absolute maximum rating can cause a CMOS circuit to latch up. Elevated supply voltage may cause internal junctions to break down, producing substrate current capable of triggering latchup. Latchup is just one of the reasons overvoltage should be avoided; other undesirable effects may result from this.

Overshoot/Undershoot

Generally the I/O pins experience the noisiest electrical environment. Fast switching signals with a large capacitive load may overshoot, creating a transient forward bias condition at the I/O junction. These junction diodes are illustrated in Figures 3 and 4. Typically this is where latchup is most likely to be induced. Proper design of the input and output buffers is essential to minimize the risk of latchup due to overshoot.

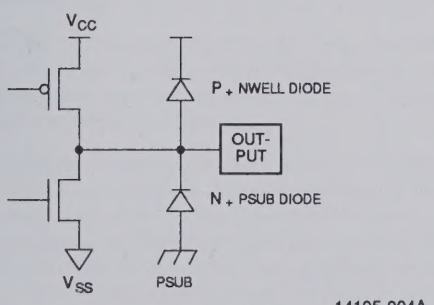


Figure 3

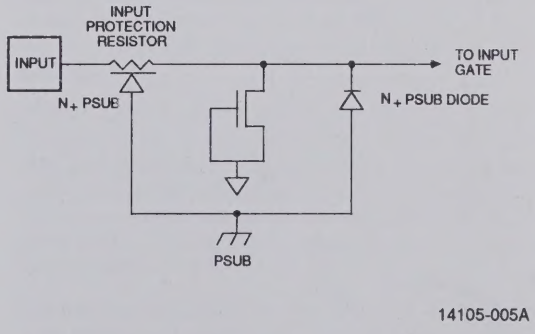


Figure 4

Testing For Latchup

Advanced Micro Devices characterizes the latchup sensitivity of its devices before they are released to the market. Testing is done in such a way as to completely cover every possible latchup condition, including V_{CC} overvoltage, pin overcurrent, and pin overvoltage.

V_{CC} Overvoltage Test

The V_{CC} overvoltage test is applied to all power (V_{CC}) pins. The test is performed at the highest guaranteed operating temperature of the device. All inputs and I/Os acting as inputs are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open).

V_{CC} max is applied to the V_{CC} pin. A positive high voltage pulse is then applied to the V_{CC} pin and returned to V_{CC} max. The occurence of latchup is detected if the voltage across the device is less than V_{CC} max, and the current through the device is greater than the normal DC operating current.

Pin Overcurrent Test

The pin overcurrent test is performed on every output, I/O pin, and non-current-limited input pin. Non-current-limited inputs are inputs which present a diode-like (or otherwise "infinite") current characteristic for input voltages in the range (GND – 5 V) < Vin < (V_{CC} + 5 V).

The pin overcurrent test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs should be floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. A three-state output under test should be disabled. A non-three-state output type under test should be a logic High when applying a positive current and a logic Low when applying a negative current. An I/O pin should be placed into the input mode.

A high current pulse is then applied to the pin under test. The magnitude of the pulse is stepped until latchup is induced. Both positive and negative currents are tested. Latchup is observed as described previously. The sensitivity of the device is the worst case sensitivity found on any pin of the device.

Pin Overvoltage Test

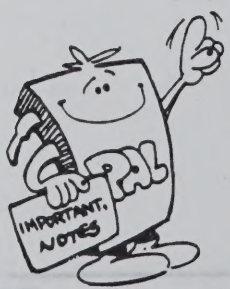
The pin overvoltage test is performed on current-limited inputs. Current-limited inputs are inputs which present a resistor-like (or otherwise "limited") current characteristic for input voltages in the range (GND – 5 V) < Vin < (V_{CC} + 5 V).

The pin overvoltage test is performed at the highest guaranteed operating temperature of the device. Input pins and I/O pins acting as inputs (which are not under test) are tied to ground or V_{CC} depending on the device logic, and outputs and I/Os acting as outputs are floating (open). V_{CC} max is applied to the V_{CC} pin.

One pin is tested at a time. Both positive and negative voltage pulses are applied to the pin under test. Latchup is observed as described previously. The sensitivity of the device is the worst-case sensitivity found on any pin of the device.

CHAPTER 5
Appendices

Glossary 5–3
Worldwide Application Support 5–10


PAL
IMPORTANT NOTES

10KH (adj.) A family of ECL devices. Circuits are temperature compensated. See also: ECL, 100K, temperature compensation.

100K (adj.) A family of ECL devices. Circuits are both temperature and voltage compensated. They have lower power dissipation and higher speed than their 10KH counterparts. See also: ECL, temperature compensation, voltage compensation, power dissipation, 10KH.

A

active high (adj.) See polarity.

active low (adj.) See polarity.

ALS (adj.) Advanced Low-power Schottky TTL family. Characterized as a lower power version of the AS family, and actually faster and lower power than the LS family. See also: AS, LS, TTL, Schottky TTL.

AND 1. (adj.) One of the three elementary logic functions. Result of the AND operation is true if and only if all operands are true. 2. (v.t.) To perform the AND operation.

AS (adj.) Advanced Schottky TTL family. High-speed versions of the standard Schottky TTL family. Generally use oxide isolated technology for very high speed. See also: Schottky TTL, TTL, oxide isolation.

assertive high (adj.) Same as "active high". See polarity.

assertive low (adj.) Same as "active low". See polarity.

astable (adj.) Describes a system which has no stable state. Such a system will oscillate. Astable circuits can be used to generate timing and synchronizing clock signals. See also: bistable, monostable.

asynchronous 1. (adj.) Describes a sequential logic system wherein operations are not synchronized to a common clock. 2. (adj.) Describes signals whose behavior and timing are completely unrelated to a particular clock. Such signals can either be random or based on another clock which has a different frequency. 3. (adj.) Describes a communication protocol whereby the timing of various operations is not determined by a system clock, but rather by events whose relationships are known, but whose exact timing cannot be precisely predicted. See also: sequential, clock, synchronous.

B

BCD (n.) Binary Coded Decimal. Decimal numbers in 4-bit binary.

binary (adj.) Having only two possible states, which can be variously called on/off, I/O, true/false, high/low, etc.

bipolar (adj.) One of the two basic types of transistor. In logic design, used for TTL, ECL, and I^2L families. See also: TTL, ECL, I^2L, MOS.

bistable (adj.) Describes a system which has 2 stable states. Any other state is unstable, and will eventually change to one of the stable states. A flip-flop is the most common electronic bistable circuit. See also: flip-flop, astable, monostable.

bit 1. (n.) Binary Digit. One unit of binary information 2. (n.) A measure of the storage capacity of a memory chip. See also: binary.

blank (adj.) Describes the state of a programmable cell after manufacturing, and before any programming, or, in the case of an erasable device, after erasure. Opposite of "programmed". See also: programmable cell, programmed, program, erase.

buffer (n.) A logic gate which performs the logic identify function; i.e., the input is passed through unchanged. Used to isolate various parts of a system, or to provide voyage or current amplification.

C

chip (n.) A single piece of semiconductor material which contains an integrated circuit. Sometimes called a die if not in a package. See also: integrated circuit, die, package.

clock 1. (adj.) A signal used to synchronize the operation of a system. 2.(adj.) An input to a clocked flip-flop. The flip-flop will not change state until an appropriate pulse appears at the clock input. 3. (n.) A circuit which generates a clock signal. 4. (v.t.) To pulse the clock signal or the clock input of a clocked flip-flop. See also: flip-flop, clocked flip-flop.

clocked flip-flop (n.) A flip-flop that does not change state until a clock signal is received. See also: flip-flop, unclocked flip-flop, clock.

CMOS (n., adj.) Complementary MOS. A type of circuit which makes use of both N-channel and P-channel

MOS transistors. Many CMOS logic circuits consume no power when not actually switching. See also: MOS, NMOS, PMOS, standby power.

combinational (adj.) See combinatorial.

combinatorial (adj.) Refers to a logic circuit which implements logic functions of present input signals only. Also called combinational. See also: sequential.

complement 1. (adj). Refers to a signal which is identical to some reference signal, except that it is of opposite polarity. Opposite of "true". 2. (v.t.) To invert. See also: true, polarity, invert.

complementary (adj.) Refers to logic device outputs which implement identical logic functions, but with opposite polarities. Used on some PLDs and ECL devices. See also: polarity, PLD, ECL.

D

decimal (adj.) Based on the number 10.

die (n.; plural: dice) Same as a chip, particularly before being placed in a package. See also: chip, package.

digit (n.) Any number from 0 to 9.

DIP (n.) Dual In-line Package. The most common integrated circuit package. It is rectangular in shape, with widths ranging from .300 inch to .900 inch, and has vertical leads along the length. See also: integrated circuit, package.

disable 1. (v.t.) To turn off a three-state output. 2. (v.t.) To inhibit another function, such as "disabling the clock". See also: three-state, enable.

download 1. (v.t.) To pass data from one machine to a less complex machine. 2. (n.) The act of downloading data. See also: upload.

E

ECL (n., adj.) Emitter Coupled Logic family. An extremely high-speed family of bipolar logic and memory devices. See also: bipolar.

EE cell (E^2 cell) (n.) A floating gate cell which can be both programmed and erased with electrical signals.

EEPROM (n.) Electrically Erasable Programmable Read-Only Memory. A nonvolatile read-only memory device which can be erased and reprogrammed, both with special electrical signals. See also: program, erase, EPROM, PROM, ROM, RAM, nonvolatile.

enable 1. (v.t.) To turn on a three-state output. 2. (adj.) By itself, usually refers to a pin which is used to enable a three-state output. Also called "output enable". 3. (adj.) Used with other function names, indicates a qualifier or inhibitor of the function. For example, "clock enable" is a function which qualifies the clock function. 4. (v.t.) To allow a signal which has been disabled to function; for example, "enabling the clock" removes any restraint which may disable the clock signal. See also: three-state, disable.

EPROM (n.) Erasable Programmable Read-Only Memory. A non-volatile read-only memory device which can be erased and reprogrammed. Erasure is accomplished by exposing the die to ultraviolet light for a period of time. Die must be packaged in a windowed package to allow erasure. See also: program, erase, EEPROM, PROM, ROM, RAM, non-volatile, windowed package.

erase 1. (v.t.) To return a programmed device to its blank state. Opposite of "program". 2. (v.t.) To return an individual programmable cell to its blank state. See also: blank, programmable cell, program.

ESD (n.) Electrostatic Discharge. The natural physical event of the transferring of electrical charges. If uncontrolled, ESD can destroy or degrade both CMOS and bipolar semiconductor devices with inadequate on-chip protection circuitry and/or insufficient packaging and handling protection. See also: ESDS Device, CMOS, bipolar.

ESDS Device (n.) Electrostatic Discharge Sensitive Device. A device which is sensitive to damage at certain levels of ESD. Three classes exist at ESD levels of up to 1999 V, to 3999 V and above 4000 V. See also: ESD.

F

finite state machine (FSM) (n.) A machine which can be in one of a finite number of states. Often used for logic circuits which sequence through various states. Such a circuit is referred to as sequential. See also: sequential.

flip-flop (n.) A bistable digital circuit. The simplest variety is called an S-R flip-flop. Other types are J-K,T, and D-type. May be unclocked or clocked. See also: bistable, unclocked flip-flop, clocked flip-flop.

floating gate (n.) A gate on an MOS transistor which is not connected to anything. Used to store charge; forms the basis of UV cells and EE cells. See also: MOS, gate, UV cell, EE cell.

FPGA 1. (n.) Field Programmable Gate Array. A high-density PLD with multiple levels of logic and programmable interconnect. 2. (n.) Field Programmable Gate Array. An array of logic gates whose configuration can be programmed by the customer. The gates are often NAND gates, but can also be NOR gates. See also: gate, program, NAND, NOR.

FPLA (n.) Field Programmable Logic Array. See PLA.

FPLS (n.) Field Programmable Logic Sequencer. A programmable logic device which is intended for sequencing or state machine applications. See also: finite state machine.

functionally complete (adj.) Refers to a logic operation or group of operations from which any complex logic function can be built. The NAND and NOR operators are functionally complete. See also: NAND, NOR.

fuse (n.) As used in programmable logic, usually refers to a lateral metal link fuse. See also: lateral fuse.

fuse map (n.) A graphic representation of the contents of a PLD. The state of each connection (fuse or other programmable cell) is represented, usually with "X" indicating an intact connection, and "-" indicating an open connection. See also: PLD, programmable cell.

G

gate 1. (n.) A fundamental logic element. The elementary gates provide NOT, AND, and OR logic functions. 2. (n.) The control terminal of a gated D-type latch. See also: latch, gated latch.

gate array (n.) A logic device which consists of an array of logic gates (usually NAND) which can be interconnected during fabrication. A custom metallization pattern is used to configure the desired functions. See also: gate, NAND, metallization.

gate equivalency (n.) A rough measure of the complexity of a digital logic integrated circuit. Indicates the approximate number of discrete logic gates that would be needed to implement the same function. See also: gate.

gated latch (n.) Generally refers to an unclocked D-type flip-flop which has a control signal called a gate. When the gate is "open", the flip-flop output follows the data input. When the gate is "closed", the output holds its current state. Also called a transparent latch. See also: flip-flop, unclocked flip-flop, gate, latch.

H

HAL® device (n.) Hard Array Logic device. A version of a PAL device which is configured during fabrication with a custom metallization pattern. HAL is a registered trademark of Advanced Micro Devices. See also: PAL device, metallization.

I

I^2L (IIL) (n., adj.) Integrated Injection Logic. A less common bipolar logic design technique which, when used, is found primarily in portions of LSI and VLSI circuits. See also: bipolar, LSI, VLSI.

integrated circuit (n.) An electronic device which has many transistors and other semiconductor components integrated onto one piece of silicon. Often abbreviated IC.

invert (v.t.) To perform the logical NOT function on a digital signal. To reverse the polarity of a digital signal. See also: polarity, NOT.

inverter (n.) A logic gate which performs logical inversion, or the NOT operation. See also: gate, NOT.

I/0 (Input/Output) 1. (n.) The methods and equipment used to pass information into and/or out of a system or device. 2. (adj.) On a programmable logic device, a pin which can function as an input and/or an output.

J

JEDEC 1. (n.) Joint Electronic Device Engineering Council. A council which creates, approves, arbitrates, and/or oversees industry standards for electronic devices. 2. (adj.) In programmable logic, refers to a computer file containing information about the programming of a device. The file format is a JEDEC-approved standard. Used for downloading to programmers. See also: program, programmer, download.

junction isolation (n.) A bipolar integrated circuit fabrication technique which uses P-N functions to isolate transistors. This is the original integrated circuit technology, and is being supplanted by oxide isolation in places where speed is critical. See also: oxide isolation, bipolar.

K

Karnaugh map (K-map) (n.) A graphic tool for minimizing sum-of-products or product-of-sums logic functions. Useful for up to six logic variables. See also: sum-of-products, product-of-sums.

L

latch 1. (n.) A type of flip-flop. Means different things to different people. In general, an unclocked flip-flop. Sometimes used to refer specifically to a gated D-type flip-flop. 2. (v.t.) To capture a signal in a latch. See also: flip-flop, unclocked flip-flop, gate, gated latch.

latch up (v.t.) To enter the latch-up condition. See also: latch-up.

latch-up (n.) A condition in which a circuit draws uncontrolled amounts of current, and certain voltages are forced, or "latched-up" to some level. Used especially in reference to CMOS devices, which can latch up if the operating conditions are violated. See also: CMOS, latch up.

lateral fuse (n.) A thin metal link which is disconnected when programmed. Connected in the blank state, disconnected in the programmed state. Usually just called a "fuse". See also: program, programmed, blank.

LCC (n.) Leadless Chip Carrier. A ceramic integrated circuit package having no leads. Connection is made to metal contacts which are flush with the package. See also: integrated circuit, lead, package.

lead (n.) [lēd] A metal conductor which provides a connection from the inside of an integrated circuit package to the outside world for soldering or other mounting techniques. See also: integrated circuit.

logic array (n.) Generally an array of programmable cells which attach inputs to logic gates of a specified type. See also: program, gate, programmable cell.

logic simulation (n.) A means whereby a logic design can be evaluated on a computer before actually being built. The computer simulates the behavior of the components to predict the behavior of the overall circuit.

LS (adj.) Low-power Schottky TTL family. Lower power version of the standard Schottky TTL family. See also: TTL, Schottky TTL.

LSI (adj.) Large-Scale Integration. A rough measure of the complexity of a digital circuit. Characterized as having 100–5000 gate equivalents for logic chips, or 1 K–16 K bits for memory chips. See also: gate equivalent, bit, VLSI, SSI, MSI.

M

macrocell (n.) Typically the output cell of a PLD, containing a flip-flop and path multiplexers.

maxterm (n.) A sum in the canonical product-of-sums form. Each maxterm contains every input variable, in either true or complemented form. See also: product-of-sums, true, complement.

metallization (n.) The process of connecting the various elements of an integrated circuit or printed circuit board by placing a layer of metal over the entire wafer or board, and then selectively etching away unwanted metal. A photolithographic mask defines the pattern of connections. See also: integrated circuit, wafer, printed circuit board.

minterm (n.) A product in the canonical sum-of-products form. Each minterm contains every input variable, either in true or complemented form. See also: sum-of-products, true, complement.

monolithic (adj.) In the electronics industry, refers to a circuit which has been integrated onto one semiconductor chip. Integrated circuits are monolithic by definition. See also: integrated circuit.

monostable (adj.) Describes a system which has 1 stable state. Any other state is unstable, and will eventually change to the stable state. The most common monostable circuit is a "one-shot". See also: bistable, astable.

MOS (n., adj.) Metal-Oxide-Semiconductor transistor. One of the two basic types of transistor. In logic design, used for NMOS, PMOS, and CMOS families. See also: NMOS, PMOS, CMOS, bipolar.

MSI (adj.) Medium-Scale Integration. A rough measure of the complexity of a digital logic circuit. Characterized as having 10–100 gate equivalents. See also: gate equivalent, SSI, LSI, VLSI.

N

NAND (adj.) Not AND. A commonly used logic gate which is equivalent to an AND gate followed by an inverter. The NAND logic operation is functionally complete.See also: gate, inverter, functionally complete, AND.

negative logic (n.) A physical implementation of logic wherein a low voltage level represents a logic 1, or "true", and a high voltage level represents a logic 0, or "false". See also: positive logic, polarity.

NMOS (n., adj.) N-channel MOS. A type of circuit which makes exclusive use of N-channel MOS transistors. See also: MOS, PMOS, CMOS.

non-volatile (adj.) Refers to memory devices which do not lose their contents when power is removed. See also: volatile.

NOR (adj.) Not OR. A logic gate which is equivalent to an OR gate followed by an inverter. The NOR logic operation is functionally complete. See also: gate, inverter, functionally complete, OR.

NOT (adj.) One of the three elementary logic functions. Unary operation whose result is true if and only if the operand is false.

O

OR 1. (adj.) One of the three elementary logic functions. Result of the OR operation is false if and only if all operands are false. 2. (v.t.) To perform the OR operation.

OTP (adj.) One-Time Programmable. Refers to programmable devices which are UV-erasable, but which are not packaged in windowed packages. As a result, there is no way to erase the device, making it programmable only once. See also: program, erase, UV-erasable, windowed package.

oxide isolation (n.) A bipolar integrated circuit fabrication technique which uses silicon oxide to isolate transistors. This results in higher speed and density. See also: junction isolation, bipolar.

P

package (n.) The encasement which protects a die and provides convenient electrical contact to the die. Materials used are generally ceramic or plastic compounds. There are a variety of shapes and sizes. See also: die.

PAL® device (n.) Programmable Array Logic device. A PLD which implements logic via a programmable AND logic array driving a fixed OR logic array. PAL is a registered trademark of Advanced Micro Devices. See also: program, logic array, sum-of-products, PLD, AND, OR.

PLA (n.) Programmable Logic Array. A programmable logic device which implements sum-of-products logic via a programmable AND logic array driving a programmable OR logic array. See also: program, logic array, sum-of-products, AND, OR.

PLCC (n.) Plastic Leaded Chip Carrier. A molded plastic integrated circuit package with leads shaped like a "J" (J-leads). Intended for surface mounting. See also: integrated circuit, lead, surface mounting, package.

PLD (n.) Programmable Logic Device. Generic term for a logic device whose function can be configured by the customer after purchase. See also: program.

PMOS (n., adj.) P-channel MOS. A type of circuit which makes exclusive use of P-channel MOS transistors. See also: MOS, NMOS, CMOS.

polarity (n.) Specifies the sense of "active" and "inactive", or "true" and "false" in a digital signal. "Active high" represents "true" as a high signal; "active low" represents "true" as a low signal.

positive logic (n.) A physical implementation of logic wherein a high voltage level represents a logic 1, or "true", and a low voltage level represents a logic 0, or "false". See also: negative logic, polarity.

power dissipation (n.) The amount of electrical power used by a device. Calculated as the product of the operating voltage and current. Measured in watts (W) or milliwatts (mW), as appropriate. Sometimes incorrectly used to refer to the operating current only.

printed circuit board (PC board, PCB) (n.) A board for assembling electrical components. Component connections are made by metal traces which have been fabricated through a metallization process. See also: trace, metallization.

product-of-sums (POS) (adj.) A representation of a logic function where the input signals are individually inverted (if necessary), then ORed together to form sums which are ANDed together. Any combinatorial logic function can be represented in product-of-sums form. See also: sum-of-products, combinatorial, AND, OR.

product term (pterm, p-term) (n.) An AND gate in a PLD which implements sum-of-products logic. See also: sum-of-products, PLD, AND, gate.

product term sharing (n.) See product term steering.

product term steering (n.) A means whereby product terms in a PAL device can be routed to one of two device outputs, instead of being dedicated only to one output. Sometimes called "product term sharing". See also: product term, PAL device.

program 1. (v.t.) As used in programmable logic, to configure a blank device so that it can perform some desired function. Applies to memory and logic devices. Opposite of "erase". 2. (v.t.) To change an individual programmable cell from a blank state to a programmed state. See also: blank, programmable cell, programmed, erase.

programmable cell (n.) Any of a variety of cells which can be altered by applying certain electrical signals. Various types are lateral and vertical fuses, UV cells, E^2 cells, and even RAM cells. All but RAM cells are non-volatile. See also: lateral fuse, vertical fuse, UV cell, E^2 cell, RAM cell, non-volatile, volatile.

programmed (adj.) Describes the state of a programmable cell or device after programming. Opposite "blank".

programmer (n.) A device or machine used for configuring, or "programming", PLDs or PROMs. See also: program, PLD, PROM.

PROM (n.) Programmable Read-Only Memory. A non-volatile memory device whose contents are programmed by the customer. Once programmed, it cannot be erased. Also functions as a PLD with a fixed AND logic array which drives a programmable OR logic array. See also: program, erase, EEPROM, EPROM, ROM, RAM, non-volatile, AND, OR, logic array.

R

RAM (n.) Random-Access Memory. Sometimes called read/write memory. A type of memory device which can be written to and read at any time. Such memory is volatile. Actually a misnomer, since most types of memories can be accessed randomly. The distinguishing feature is the fact that RAM is designed specifically to be written to in normal usage. See also: ROM, volatile.

RAM cell (n.) A cell which is used make one bit of volatile memory in a RAM. Can also form the basis of a programmable logic connectivity array. See also: RAM, volatile.

ROM (n.) Read-Only Memory. A nonvolatile memory device which has its contents defined when manufactured. No changes can be made to the memory contents. See also: PROM, EPROM, EEPROM, RAM, nonvolatile.

S

Schottky TTL (adj.) Family of TTL devices which make use of Schottky diodes for higher speed. See also: TTL.

security fuse (n.) A PLD feature which allows a user to "secure" the PLD after programming. This prevents subsequent copying of the contents of the PLD. See also: PLD, program.

semicustom (adj.) Refers to a circuit which has been partially designed by the device vendor, and partially designed, or configured, by the customer. Primary types are PLDs, gate arrays, and standard cell circuits. See also: PLD, gate array, standard cell.

sequential (adj.) Refers to a logic circuit whose operation depends both on present input signals and previous operations, or states. Requires some kind of memory (usually flip-flops) for remembering past states. See also: flip-flop, combinatorial.

SSI (adj.) Small Scale Integration. A rough measure of the complexity of a digital logic circuit. Characterized as having less than 10 gate equivalents. See also: gate equivalent, MSI, LSI, VLSI.

standard cell (n.) A method of designing semicustom or full custom circuits whereby predefined cells are brought together to provide the specified function. Unlike gate arrays, all fabrication steps are customized, instead of just the metallization step. See also: semicustom, gate array, metallization.

standby power (n.) The power consumed by a device when none of the device inputs are switching. Usually used in reference to CMOS devices, many of which consume practically no standby power. See also: CMOS.

sum-of-products (SOP) (adj.) A representation of a logic function where the input signals are individually inverted (if necessary), then ANDed together to form products which are ORed together. Any combinatorial logic function can be represented in sum-of-products form. See also: product-of-sums, combinatorial, AND, OR.

surface mounting (n.) A printed circuit board assembly technique whereby the integrated circuit packages are placed on the board with no leads protruding through to the other side. Packages can thus be mounted on both sides of the board. See also: printed circuit board, lead, through-hole mounting.

synchronous 1. (adj.) Describes a sequential logic system wherein all operations are synchronized to a common clock. 2. (adj.) Describes signals whose behavior and timing are synchronized to a clock. 3. (adj.) Describes a communication protocol whereby the timing of various operations is determined by a system clock. See also: sequential, clock, asynchronous.

T

temperature compensation (n.) A circuit feature which allows some electrical characteristics to remain relatively constant with some variation in operating temperature.

three-state (adj.) A type of logic device output which can be in one of three-states: HIGH, LOW, and OFF, or High-Z (high impedance). When enabled (on), performs as a normal binary output. When disabled (off), acts as an open pin. See also: enable, disable, binary.

through-hole mounting (n.) A printed circuit board assembly technique whereby the leads of the various components extend through holes in the board. These leads are then soldered from the opposite side of the board. See also: printed circuit board, lead, surface mounting.

trace 1. (n.) During logic simulation, the behavior of a signal or group of signals. The results can sometimes be stored in a "trace file" on disk for later analysis. 2. (n.) A thin layer of metal on a printed circuit board which provides connections between components. Performs the function of a wire. See also: logic simulation, printed circuit board.

transparent latch (n.) See gated latch.

TRI-STATE® (adj.) See three-state. TRI-STATE is a registered trademark of National Semiconductor Corp.

true (adj.) Refers to a signal which is identical to some reference signal, with the same polarity. Opposite of "complement". See also: complement, polarity.

TTL (adj.) Transistor-Transistor Logic family. The most widely used family of bipolar logic devices. The name refers to the particular circuit design technique used. See also: bipolar.

U

unclocked flip-flop (n.) A flip-flop that changes state as soon as the appropriate controls are applied.See also: flip-flop, clocked flip-flop.

upload 1. (v.t.) To pass data from one machine to a more complex machine. 2. (n.) The act of uploading data. See also: download.

UV cell (n.) A floating gate cell which can be erased by exposure to ultraviolet (UV) light. See also: floating gate, erase.

UV-erasable (adj.) Refers to devices or programmable cells which can be erased when exposed to ultraviolet (UV) light for a period of time. See also: programmable cell, erase.

V

vertical fuse (n.) A transistor arranged such that the emitter and base are shorted together when programmed. Disconnected in the blank state, connected in the programmed state. See also: program, programmed, blank.

VLSI (adj.) Very Large Scale Integration. A rough measure of the complexity of a digital circuit. Characterized as having 5000 or more gate equivalents for logic chips, or 16K or more bits for memory chips. See also: gate equivalent, bit, SSI, MSI, LSI.

volatile (adj.) Refers to memory devices which lose their contents when power is removed. See also: nonvolatile.

voltage compensation (n.) A circuit feature which allows some electrical characteristics to remain relatively constant with some variation in the supply voltage.

W

wafer (n.) A round slice of very pure silicon which is used in the fabrication of integrated circuits. Several circuits can be built on one wafer. See also: integrated circuit.

windowed package (n.) A package which has a quartz window in the lid directly over the die. This makes it possible to expose the die to ultraviolet light for erasing the device.See also: erase, die, package.

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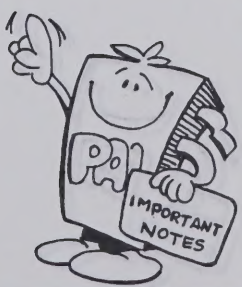
14111	A	/0	1/92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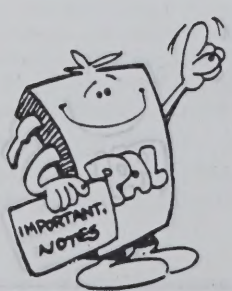
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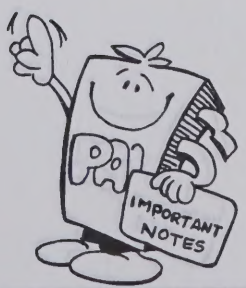
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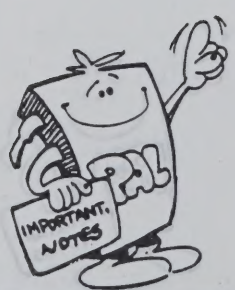
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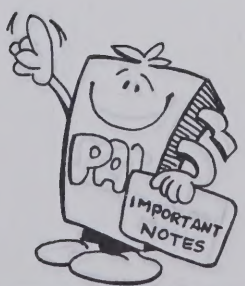
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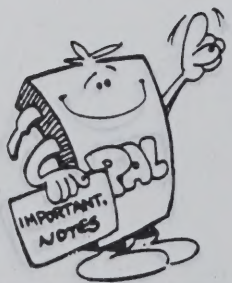
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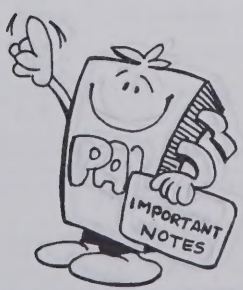
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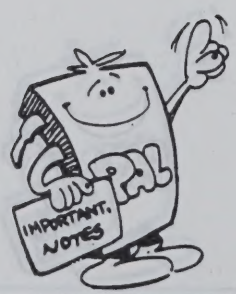
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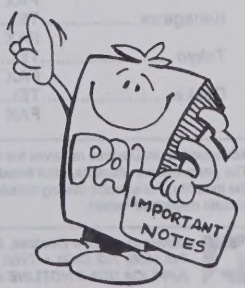
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	PAL16L8-5 PAL16R8-5 PAL16R6-5 PAL16R4-5	20P, J	TTL	5	210	
	PAL16L8-7 PAL16R8-7 PAL16R6-7 PAL16R4-7	20P, J	TTL	7.5	180	
	PAL16L8D PAL16R8D PAL16R6D PAL16R4D	20N, J	TTL	10	180	
	PAL16L8B PAL16R8B PAL16R6B PAL16R4B	20N, J	TTL	15	180	
	PAL16L8B-2 PAL16R8B-2 PAL16R6B-2 PAL16R4B-2	20N, J	TTL	25	90	
	PAL16L8A PAL16R8A PAL16R6A PAL16R4A	20N, J	TTL	25	180	
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	PAL20L8B PAL20R8B PAL20R6B PAL20R4B	24NS, 28NL	TTL	15	210	
	PAL20L8B-2 PAL20R8B-2 PAL20R6B-2 PAL20R4B-2	24NS, 28FN	TTL	25	105	
	PAL20L8A PAL20R8A PAL20R6A PAL20R4A	24NS, 28NL	TTL	25	210	

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